DGN–8 D–8

SGLS270B – DECEMBER 2004 – REVISED JULY 2008

LOW NOISE, HIGH SLEW RATE, UNITY GAIN STABLE VOLTAGE FEEDBACK AMPLIFIER

FEATURES

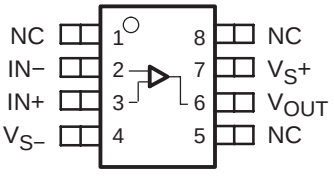
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of −55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree**(1)
- **Unity Gain Stability**
- **Low Voltage Noise**
  - **3 nV/$\sqrt{\text{Hz}}$**
- **High Slew Rate: 1000 V/μs**
- **Low Distortion**
  - **−92 dBc THD at 30 MHz**
- **Wide Bandwidth: 1.4 GHz**
- **Supply Voltages**
  - **+5 V, ±5 V, +12 V, +15 V**
- **Power Down Functionality (THS4275)**
- **Evaluation Module Available**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

APPLICATIONS

- **High Linearity ADC Preamplifier**
- **Wireless Communication Receivers**
- **Differential to Single-Ended Conversion**
- **DAC Output Buffer**
- **Active Filtering**

THS4271



DESCRIPTION

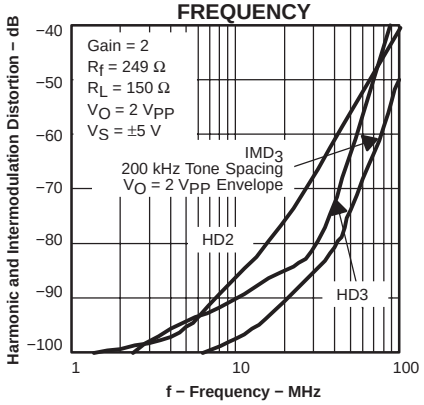
The THS4271 and THS4275 are low-noise, high slew rate, unity gain stable voltage feedback amplifiers designed to run from supply voltages as low as 5 V and as high as 15 V. The THS4275 offers the same performance as the THS4271 with the addition of power down capability. The combination of low-noise, high slew rate, wide bandwidth, low distortion, and unity gain stability make the THS4271 and THS4275 high performance devices across multiple ac specifications.

Designers using the THS4271 are rewarded with higher dynamic range over a wider frequency band without the stability concerns of decompensated amplifiers. The devices are available in SOIC, MSOP with PowerPAD™, and leadless MSOP with PowerPAD™ packages.

RELATED DEVICES

DEVICE	DESCRIPTION
THS4211	1-GHz voltage feedback amplifier
THS4503	Wideband fully differential amplifier
THS3202	Dual, wideband current feedback amplifier

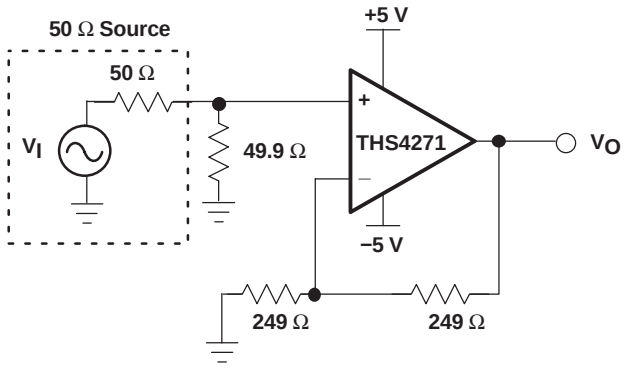
HARMONIC AND INTERMODULATION DISTORTION vs FREQUENCY



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

Low-Noise, Low-Distortion, Wideband Application Circuit



NOTE: Power supply decoupling capacitors not shown

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UNIT
Supply voltage, V_S		16.5 V
Input voltage, V_I		$\pm V_S$
Output current, I_O		100 mA
Continuous power dissipation	See the Dissipation Rating Table	
Maximum junction temperature, T_J		150°C
Maximum junction temperature, continuous operation, long term reliability T_J (2)		125°C
Storage temperature range, T_{stg}		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C
ESD ratings:	HBM	3000 V
	CDM	1000 V
	MM	100 V

(1) The absolute maximum temperature under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See Figure 1 for additional information on thermal derating.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA}(1) (°C/W)
D (8 pin)	38.3	97.5
DGN (8 pin)(2)	4.7	58.4

(1) This data was taken using the JEDEC standard High-K test PCB.

(2) The THS4271/5 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heat sink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See Texas Instruments technical briefs SLMA002 and SLMA004 for more information about utilizing the PowerPAD thermally enhanced package.

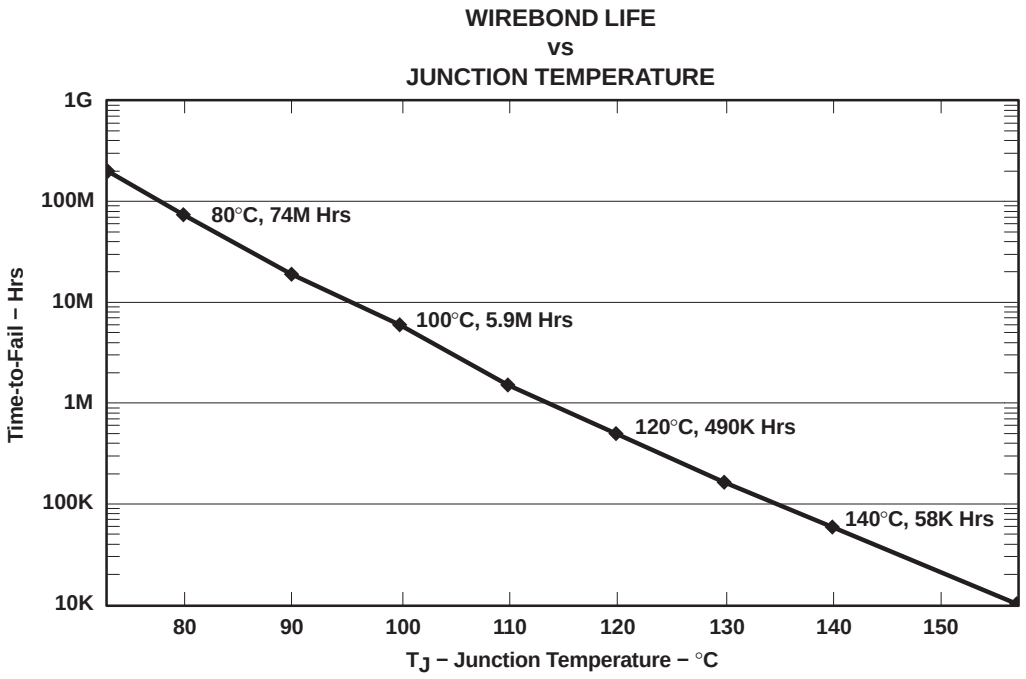


Figure 1. EME−G600 Estimated Wirebond Life

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, (V_{S+} and V_{S-})	Dual supply	±2.5	±7.5	V
	Single supply	5	15	
Input common-mode voltage range		V_{S-} + 1.4	V_{S+} − 1.4	V
Operating free-air temperature, T_A		−55	125	°C

PACKAGING/ORDERING INFORMATION

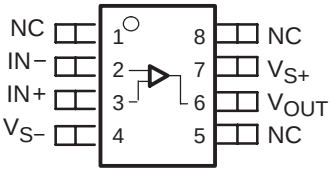
ORDERABLE PACKAGE AND NUMBER		
PLASTIC SMALL OUTLINE (D) (1)	PLASTIC MSOP (1) PowerPAD	
	(DGN)	PACKAGE MARKING
THS4271MDEP(2)	THS4271MDGNTEP(2)	BLT
THS4271MDREP(2)	THS4271MDGNREP	
THS4275MDEP(2)	THS4275MDGNTEP(2)	BLY
THS4275MDREP(2)	THS4275MDGNREP(2)	

(1) All packages are available taped and reeled. The R suffix standard quantity is 2500 (e.g., THS4271MDGNREP).
(2) Product Preview

PIN ASSIGNMENTS

(TOP VIEW) D, DGN

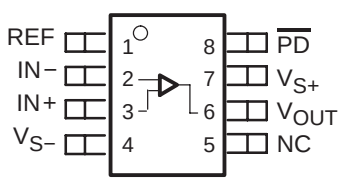
THS4271



NC − No internal connection

(TOP VIEW) D, DGN

THS4275



ELECTRICAL CHARACTERISTICS V_S = ±5 V

R_F = 301 Ω, R_L = 499 Ω, G = +2, unless otherwise noted

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE			MIN/ TYP/ MAX
		25°C	25°C	−55°C TO 125°C	UNITS	
AC PERFORMANCE						
Small signal bandwidth	G = 1, V_O = 100 mV_{PP}, R_L = 150 Ω	1.4			GHz	Typ
	G = −1, V_O = 100 mV_{PP}	400			MHz	
	G = 2, V_O = 100 mV_{PP}	390			MHz	
	G = 5, V_O = 100 mV_{PP}	85			MHz	
	G = 10, V_O = 100 mV_{PP}	40			MHz	
0.1-dB flat bandwidth	G = 1, V_O = 100 mV_{PP}, R_L = 150 Ω	200			MHz	Typ
Gain bandwidth product	G > 10, f = 1 MHz	400			MHz	Typ
Full-power bandwidth	G = −1, V_O = 2 V_p	80			MHz	Typ
Slew rate	G = 1, V_O = 2 V Step	950			V/µs	Typ
	G = −1, V_O = 2 V Step	1000				
Settling time to 0.1%	G = −1, V_O = 4 V Step	25			ns	Typ
Settling time to 0.01%	G = −1, V_O = 4 V Step	38			ns	Typ
Harmonic distortion	G = 1, V_O = 1 V_{PP}, f = 30 MHz					
Second harmonic distortion	R_L = 150 Ω	−92			dBc	Typ
	R_L = 499 Ω	−80				
Third harmonic distortion	R_L = 150 Ω	−95			dBc	Typ
	R_L = 499 Ω	−95				
Harmonic distortion	G = 2, V_O = 2 V_{PP}, f = 30 MHz					
Second harmonic distortion	R_L = 150 Ω	−65			dBc	Typ
	R_L = 499 Ω	−70				
Third harmonic distortion	R_L = 150 Ω	−80			dBc	Typ
	R_L = 499 Ω	−90				
Third order intermodulation (IMD_3)	G = 2, V_O = 2 V_{PP}, R_L = 150 Ω, f = 70 MHz	−60			dBc	Typ
Third order output intercept (OIP_3)	G = 2, V_O = 2 V_{PP}, R_L = 150 Ω, f = 70 MHz	35			dBm	Typ
Differential gain (NTSC, PAL)	G = 2, R_L = 150 Ω	0.007%				Typ
Differential phase (NTSC, PAL)	G = 2, R_L = 150 Ω	0.004			degrees	Typ
Input voltage noise	f = 1 MHz	3			nV/√Hz	Typ
Input current noise	f = 1 MHz	3			pA√Hz	Typ
DC PERFORMANCE						
Open-loop voltage gain (A_{OL})	V_O = ±50 mV, R_L = 499 Ω	75	65	56	dB	Min
Input offset voltage	V_{CM} = 0 V	5	±14	±16	mV	Max
Average offset voltage drift	V_{CM} = 0 V			±10	µV/°C	Typ
Input bias current	V_{CM} = 0 V	6	15	18	µA	Max
Average bias current drift	V_{CM} = 0 V			±10	nA/°C	Typ
Input offset current	V_{CM} = 0 V	1	6	8	µA	Max
Average offset current drift	V_{CM} = 0 V			±10	nA/°C	Typ
INPUT CHARACTERISTICS						
Common-mode input range		±4	±3.6	±3.5	V	Min
Common-mode rejection ratio	V_{CM} = ±1 V	72	67	62	dB	Min
Input resistance	Common-mode	5			MΩ	Typ
Input capacitance	Common-mode / differential	0.4/0.8			pF	Typ

ELECTRICAL CHARACTERISTICS V_S = ±5 V (CONTINUED)

R_F = 301 Ω, R_L = 499 Ω, G = +2, unless otherwise noted

PARAMETER	TEST CONDITIONS		TYP	OVER TEMPERATURE			MIN/ TYP/ MAX
			25°C	25°C	−55°C to 125°C	UNITS	
OUTPUT CHARACTERISTIC8							
Output voltage swing	G = +2		±4	±3.75	±3.6	V	Min
Output current (sourcing)	R_L = 10 Ω		160	120	104	mA	Min
Output current (sinking)	R_L = 10 Ω		80	60	44	mA	Min
Output impedance	f = 1 MHz		0.1			Ω	Typ
POWER SUPPLY							
Specified operating voltage			±5	±7.5	±7.5	V	Max
Maximum quiescent current			22	24	34	mA	Max
Minimum quiescent current			22	20	13	mA	Min
Power supply rejection (+PSRR)	V_{S+} = 5.5 V to 4.5 V, V_{S-} = −5 V		85	75	58	dB	Min
Power supply rejection (−PSRR)	V_{S+} = 5 V, V_{S-} = −5.5 V to −4.5 V		75	65	57	dB	Min
POWER-DOWN CHARACTERISTICS (THS4275 only)							
Power-down voltage level(1)	REF = 0 V, or V_{S-}	Enable		REF+1.8		V	Min
		Power down		REF+1		V	Max
	REF = V_{S+} or Floating	Enable		REF−1		V	Min
		Power down		REF−1.7		V	Max
Power-down quiescent current	PD = Ref +1 V, Ref = 0 V		875	1000	1200	µA	Max
	PD = Ref −1.7 V, Ref = V_{S+}		650	800	1000	µA	Max
Turnon time delay ($t_{(ON)}$)	50% of final supply current value		4			µs	Typ
Turnoff time delay ($t_{(OFF)}$)	50% of final supply current value		3			µs	Typ
Input impedance	f = 1 MHz		4			GΩ	Typ
Output impedance			200			kΩ	Typ

(1) For detailed information on the power-down circuit, see the *powerdown* section in the *Application Information* section of this data sheet.

ELECTRICAL CHARACTERISTICS V_S = 5 V

R_F = 301 Ω, R_L = 499 Ω, G = +2, unless otherwise noted

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE			MIN/ TYP/ MAX
		25°C	25°C	−55°C to 125°C	UNITS	
AC PERFORMANCE						
Small signal bandwidth	G = 1, V_O = 100 mV_{PP}, R_L = 150 Ω	1.2			GHz	Typ
	G = −1, V_O = 100 mV_{PP}	380			MHz	
	G = 2, V_O = 100 mV_{PP}	360			MHz	
	G = 5, V_O = 100 mV_{PP}	80			MHz	
	G = 10, V_O = 100 mV_{PP}	35			MHz	
0.1-dB flat bandwidth	G = 1, V_O = 100 mV_{PP}, R_L = 150 Ω	120			MHz	Typ
Gain bandwidth product	G > 10 , f = 1 MHz	350			MHz	Typ
Full-power bandwidth	G = −1, V_O = 2 V_p	60			MHz	Typ
Slew rate	G = 1, V_O = 2 V Step	700			V/µs	Typ
	G = −1, V_O = 2 V Step	750				
Settling time to 0.1%	G = −1, V_O = 2 V Step	18			ns	Typ
Settling time to 0.01%	G = −1, V_O = 2 V Step	66			ns	Typ
Harmonic distortion	G = 1, V_O = 1 V_{PP}, f = 30 MHz					
Second harmonic distortion	R_L = 150 Ω	−75			dBc	Typ
	R_L = 499 Ω	−72				
Third harmonic distortion	R_L = 150 Ω	−70			dBc	Typ
	R_L = 499 Ω	−70				
Third order intermodulation (IMD_3)	G = 2, V_O = 1 V_{PP}, R_L = 150 Ω, f = 70 MHz	−65			dBc	Typ
Third order output intercept (OIP_3)	G = 2, V_O = 1 V_{PP}, R_L = 150 Ω, f = 70 MHz	32			dBm	Typ
Input voltage noise	f = 1 MHz	3			nV/√Hz	Typ
Input current noise	f = 10 MHz	3			pA/√Hz	Typ
DC PERFORMANCE						
Open-loop voltage gain (A_{OL})	V_O = ± 50 mV, R_L = 499 Ω	68	63	56	dB	Min
Input offset voltage	V_{CM} = V_S/2	5	±14	±16	mV	Max
Average offset voltage drift	V_{CM} = V_S/2			±10	µV/°C	Typ
Input bias current	V_{CM} = V_S/2	6	15	18	µA	Max
Average bias current drift	V_{CM} = V_S/2			±10	nA/°C	Typ
Input offset current	V_{CM} = V_S/2	1	6	8	µA	Max
Average offset current drift	V_{CM} = V_S/2			±10	nA/°C	Typ
INPUT CHARACTERISTICS						
Common-mode input range		1/4	1.3/3.7	1.5/3.5	V	Min
Common-mode rejection ratio	V_{CM} = ±0.5 V, V_O = 2.5 V	72	67	62	dB	Min
Input resistance	Common-mode	5			MΩ	Typ
Input capacitance	Common-mode / differential	0.4/0.8			pF	Typ
OUTPUT CHARACTERISTICS						
Output voltage swing	G = +2	1.2/3.8	1.4/3.6	1.5/3.5	V	Min
Output current (sourcing)	R_L = 10 Ω	120	90	78	mA	Min
Output current (sinking)	R_L = 10 Ω	65	45	37	mA	Min
Output impedance	f = 1 MHz	0.1			Ω	Typ

ELECTRICAL CHARACTERISTICS V_S = 5 V (CONTINUED)

R_F = 301 Ω, R_L = 499 Ω, G = +2, unless otherwise noted

PARAMETER	TEST CONDITIONS		TYP	OVER TEMPERATURE			MIN/ TYP/ MAX
			25°C	25°C	−55°C to 125°C	UNITS	
POWER SUPPLY							
Specified operating voltage			5	15	15	V	Max
Maximum quiescent current			20	23	34	mA	Max
Minimum quiescent current			20	18	13	mA	Min
Power supply rejection (+PSRR)	V_{S+} = 5.5 V to 4.5 V, V_{S-} = 0 V		85	70	57	dB	Min
Power supply rejection (−PSRR)	V_{S+} = 5 V, V_{S-} = −0.5 V to 0.5 V		75	65	56	dB	Min
POWER-DOWN CHARACTERISTICS (THS4275 Only)							
Power-down voltage level(1)	REF = 0 V, or V_{S-}	Enable		REF+1.8		V	Min
		Power down		REF+1		V	Max
	REF = V_{S+} or Floating	Enable		REF−1		V	Min
		Power down		REF−1.7		V	Max
Power-down quiescent current	PD = Ref +1 V, Ref = 0 V		650	800	1000	µA	Max
	PD = Ref −1.7 V, Ref = V_{S+}		650	800	1000	µA	Max
Turnon time delay($t_{(ON)}$)	50% of final value		4			µs	Typ
Turnoff time delay ($t_{(OFF)}$)	50% of final value		3			µs	Typ
Input impedance	f = 1 MHz		6			GΩ	Typ
Output impedance			100			kΩ	Typ

(1) For detailed information on the power-down circuit, see the *powerdown* section in the *Application Information* section of this data sheet.

TYPICAL CHARACTERISTICS

Table of Graphs (±5 V)

		FIGURE
Small signal unity gain frequency response		1
Small signal frequency response		2
0.1-dB gain flatness frequency response		3
Large signal frequency response		4
Slew rate	vs Output voltage	5
Harmonic distortion	vs Frequency	6, 7, 8, 9
Harmonic distortion	vs Output voltage swing	10, 11, 12, 13
Third order intermodulation distortion	vs Frequency	14, 16
Third order intercept point	vs Frequency	15, 17
Voltage and current noise	vs Frequency	18
Differential gain	vs Number of loads	19
Differential phase	vs Number of loads	20
Settling time		21
Quiescent current	vs Supply voltage	22
Output voltage	Load resistance	23
Frequency response	vs Capacitive load	24
Open-loop gain and phase	vs Frequency	25
Open-loop gain	vs Case temperature	26
Rejection ratios	vs Frequency	27
Rejection ratios	vs Case temperature	28
Common-mode rejection ratio	vs Input common-mode range	29
Input offset voltage	vs Case temperature	30
Input bias and offset current	vs Case temperature	31
Small signal transient response		32
Large signal transient response		33
Overdrive recovery		34
Closed-loop output impedance	vs Frequency	35
Power-down quiescent current	vs Supply voltage	36
Power-down output impedance	vs Frequency	37
Turnon and turnoff delay times		38

TYPICAL CHARACTERISTICS

Table of Graphs (5 V)

		FIGURE
Small signal unity gain frequency response		39
Small signal frequency response		40
0.1-dB gain flatness frequency response		41
Large signal frequency response		42
Slew rate	vs Output voltage	43
Harmonic distortion	vs Frequency	44, 45, 46, 47
Harmonic distortion	vs Output voltage swing	48, 49, 50, 51
Third order intermodulation distortion	vs Frequency	52, 54
Third order intercept point	vs Frequency	53, 55
Voltage and current noise	vs Frequency	56
Settling time		57
Quiescent current	vs Supply voltage	58
Output voltage	vs Load resistance	59
Frequency response	vs Capacitive load	60
Open-loop gain and phase	vs Frequency	61
Open-loop gain	vs Case temperature	62
Rejection ratios	vs Frequency	63
Rejection ratios	vs Case temperature	64
Common-mode rejection ratio	vs Input common-mode range	65
Input offset voltage	vs Case temperature	66
Input bias and offset current	vs Case temperature	67
Small signal transient response		68
Large signal transient response		69
Overdrive recovery		70
Closed-loop output impedance	vs Frequency	71
Power-down quiescent current	vs Supply voltage	72
Power-down output impedance	vs Frequency	73
Turnon and turnoff delay times		74

TYPICAL CHARACTERISTICS (±5 V GRAPHS)

SMALL SIGNAL UNITY GAIN FREQUENCY RESPONSE

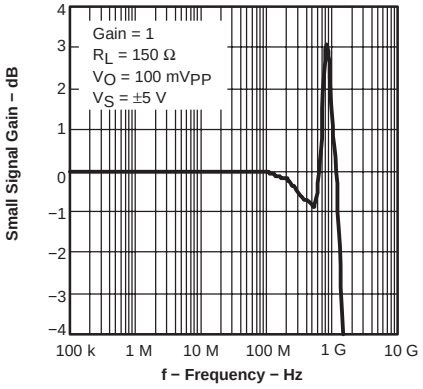


Figure 2

SMALL SIGNAL FREQUENCY RESPONSE

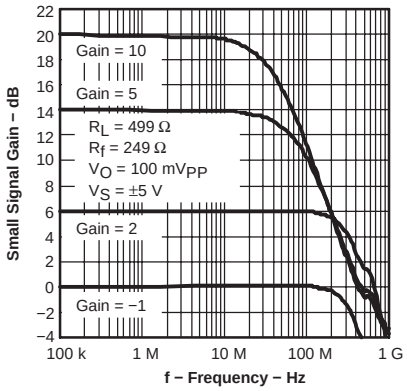


Figure 3

0.1 dB GAIN FLATNESS FREQUENCY RESPONSE

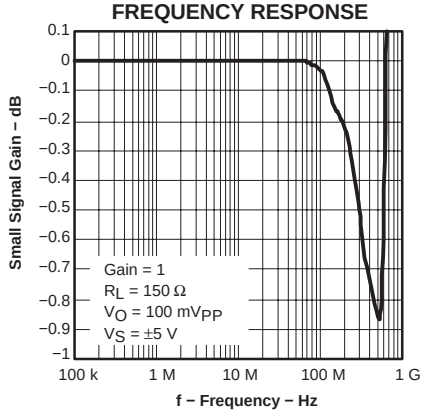


Figure 4

LARGE SIGNAL FREQUENCY RESPONSE

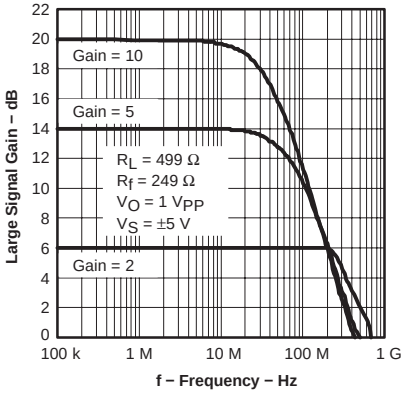


Figure 5

SLEW RATE vs OUTPUT VOLTAGE

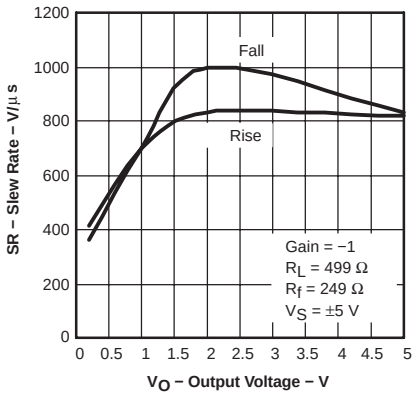


Figure 6

HARMONIC DISTORTION vs FREQUENCY

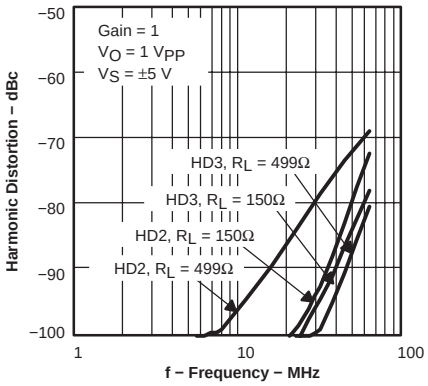


Figure 7

HARMONIC DISTORTION vs FREQUENCY

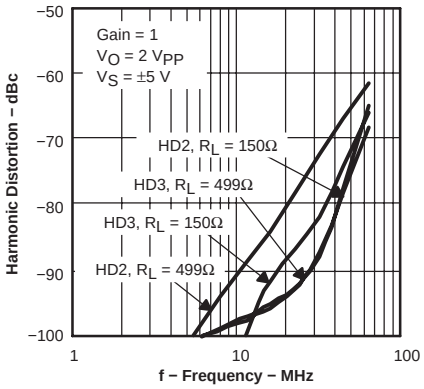


Figure 8

HARMONIC DISTORTION vs FREQUENCY

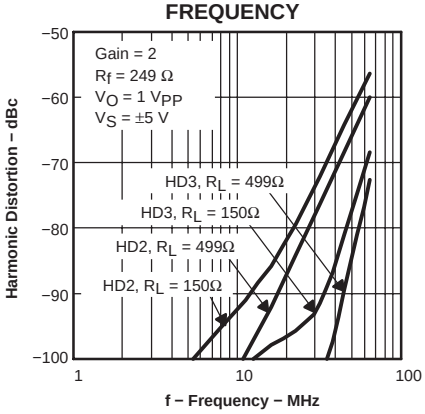


Figure 9

HARMONIC DISTORTION vs FREQUENCY

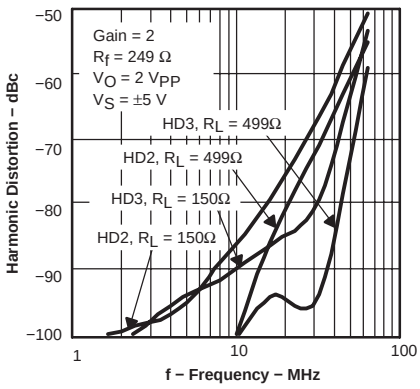


Figure 10

TYPICAL CHARACTERISTICS (±5 V GRAPHS) (CONTINUED)

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

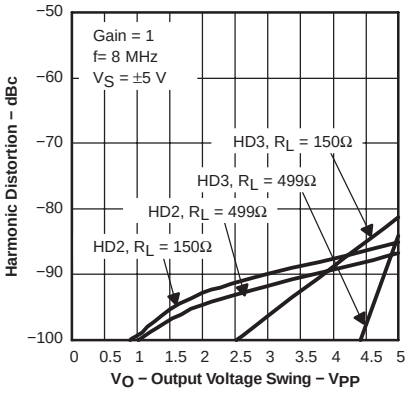


Figure 11

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

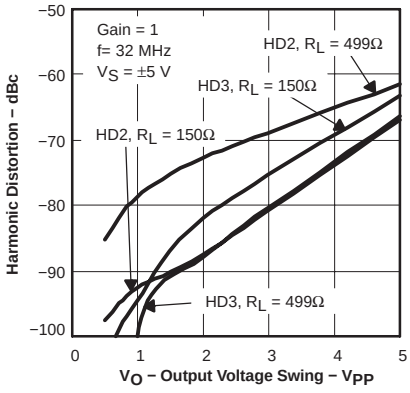


Figure 12

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

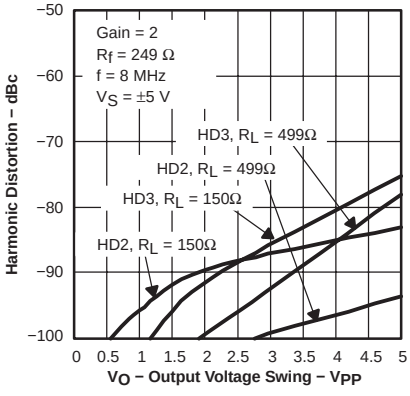


Figure 13

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

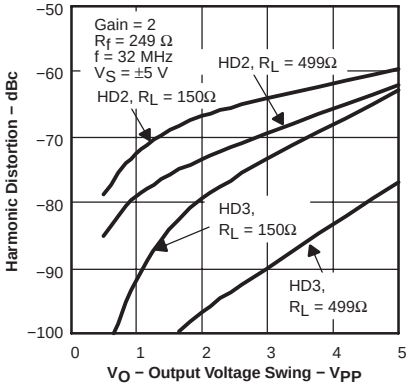


Figure 14

THIRD ORDER INTERMODULATION DISTORTION vs FREQUENCY

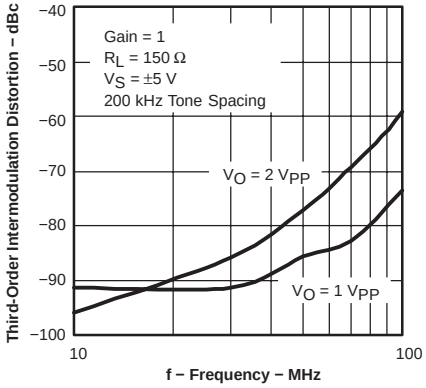


Figure 15

THIRD ORDER OUTPUT INTERCEPT POINT vs FREQUENCY

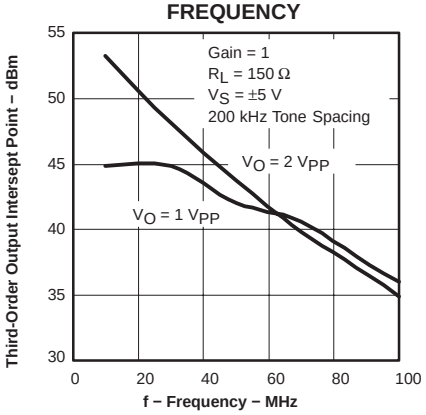


Figure 16

THIRD ORDER INTERMODULATION DISTORTION vs FREQUENCY

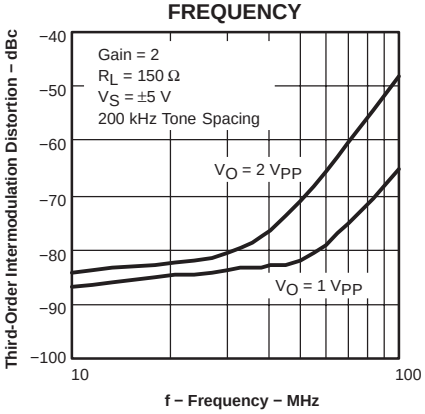


Figure 17

THIRD ORDER OUTPUT INTERCEPT POINT vs FREQUENCY

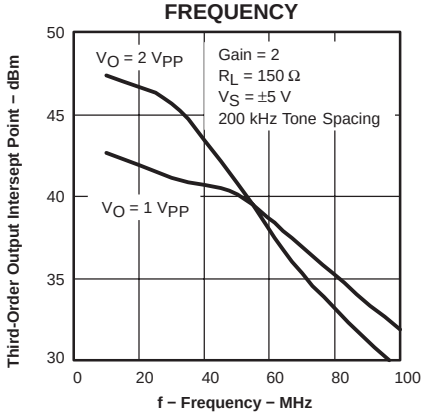


Figure 18

VOLTAGE AND CURRENT NOISE vs FREQUENCY

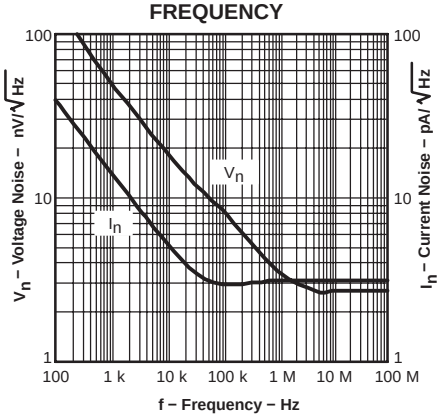


Figure 19

TYPICAL CHARACTERISTICS (±5 V GRAPHS) (CONTINUED)

DIFFERENTIAL GAIN vs NUMBER OF LOADS

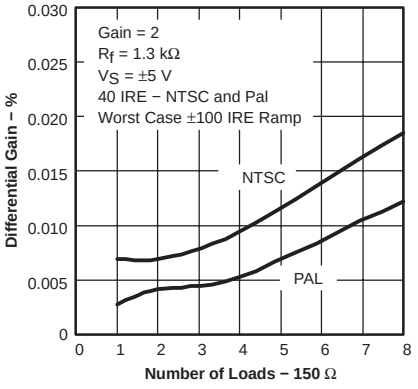


Figure 20

DIFFERENTIAL PHASE vs NUMBER OF LOADS

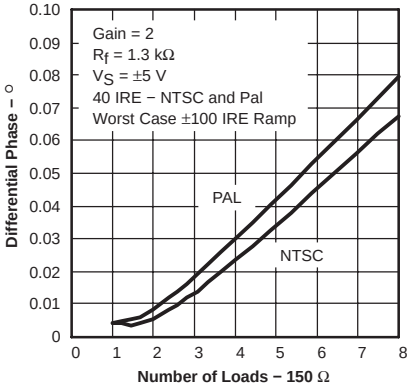


Figure 21

SETTLING TIME

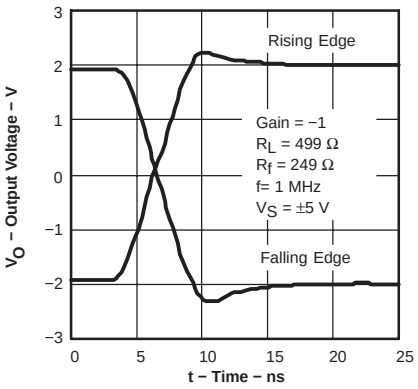


Figure 22

QUIESCENT CURRENT vs SUPPLY VOLTAGE

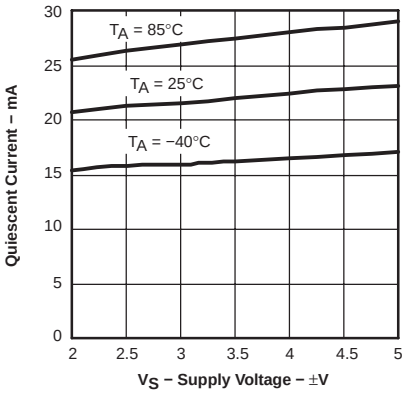


Figure 23

OUTPUT VOLTAGE vs LOAD RESISTANCE

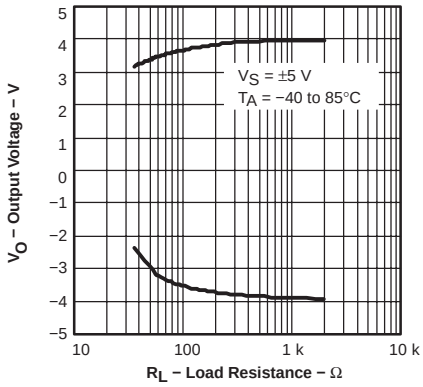


Figure 24

FREQUENCY RESPONSE vs CAPACITIVE LOAD

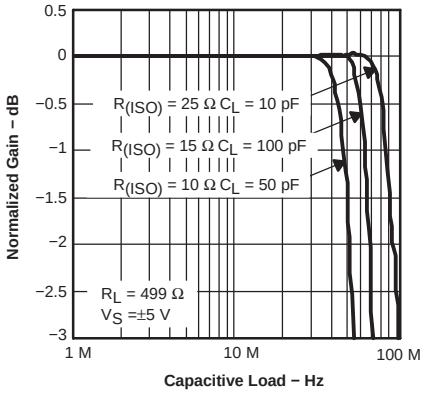


Figure 25

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

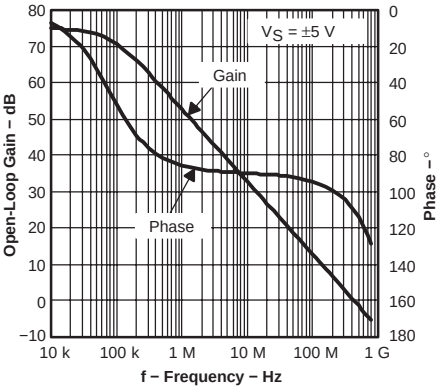


Figure 26

OPEN-LOOP GAIN vs CASE TEMPERATURE

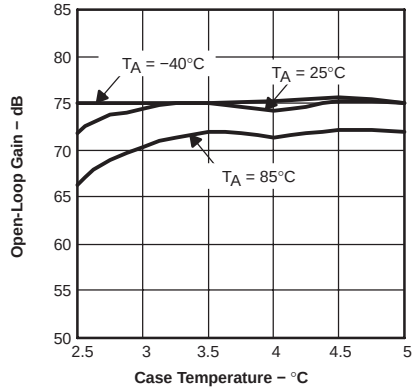


Figure 27

REJECTION RATIOS vs FREQUENCY

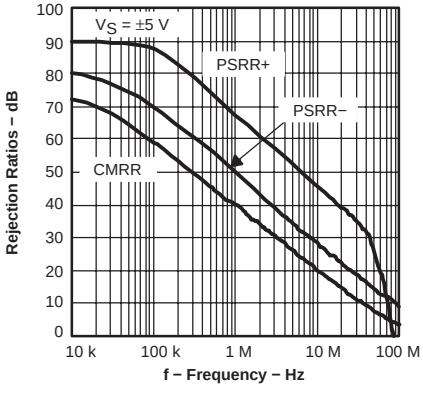


Figure 28

TYPICAL CHARACTERISTICS (±5 V GRAPHS) (CONTINUED)

REJECTION RATIOS vs CASE TEMPERATURE

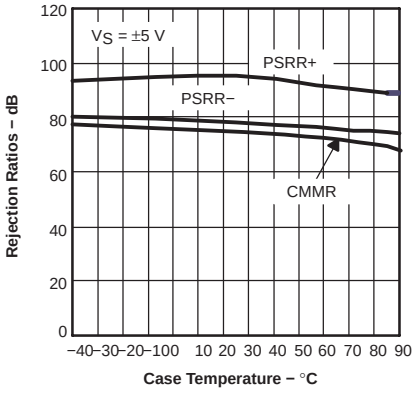


Figure 29

COMMON-MODE REJECTION RATIO vs INPUT COMMON-MODE RANGE

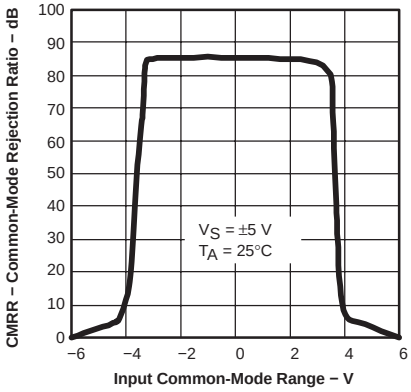


Figure 30

INPUT OFFSET VOLTAGE vs CASE TEMPERATURE

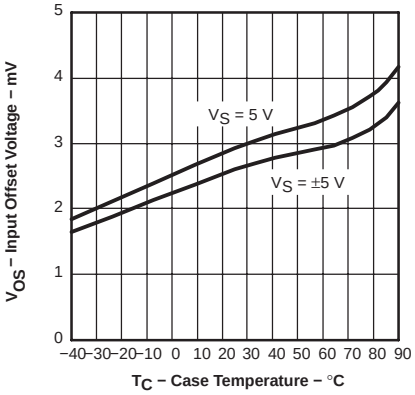


Figure 31

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

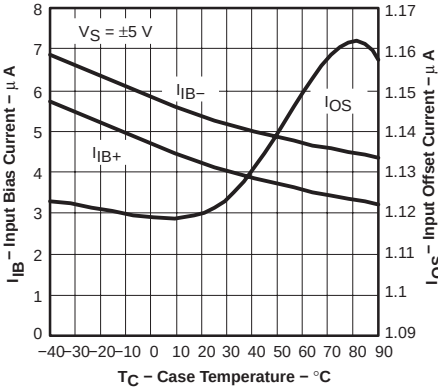


Figure 32

SMALL SIGNAL TRANSIENT RESPONSE

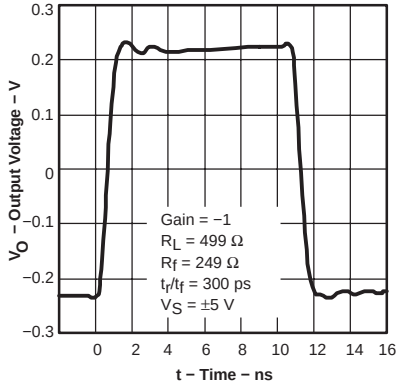


Figure 33

LARGE SIGNAL TRANSIENT RESPONSE

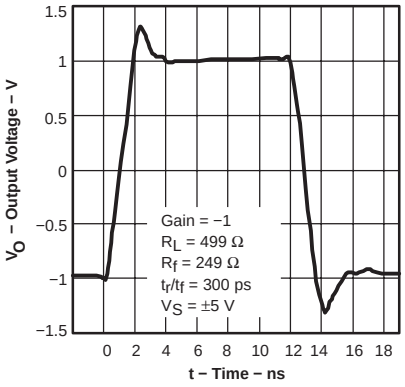


Figure 34

OVERDRIVE RECOVERY

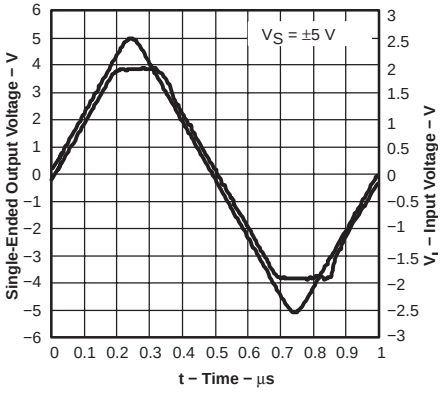


Figure 35

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

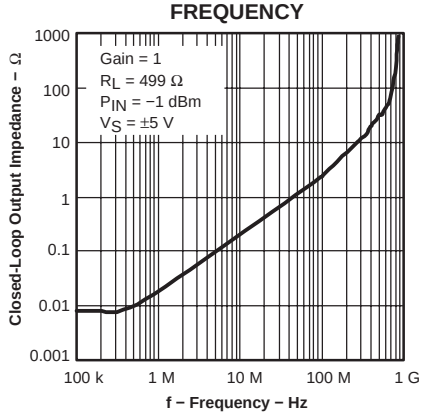


Figure 36

POWER-DOWN QUIESCENT CURRENT vs SUPPLY VOLTAGE

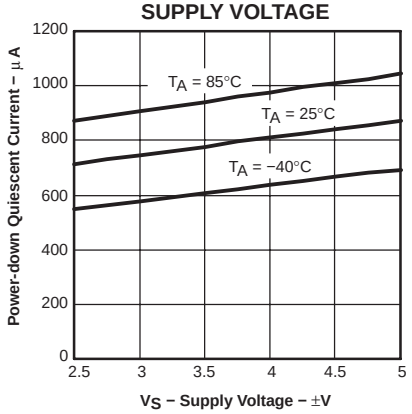


Figure 37

TYPICAL CHARACTERISTICS (±5 V GRAPHS) (CONTINUED)

POWER-DOWN OUTPUT IMPEDANCE VS FREQUENCY

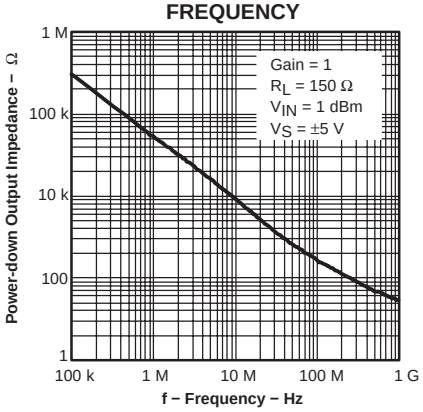


Figure 38

TURNON AND TURNOFF TIMES DELAY TIME

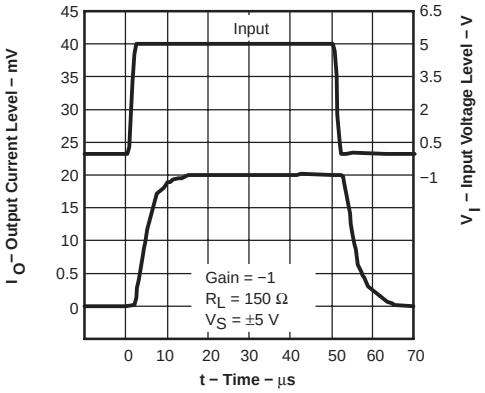


Figure 39

TYPICAL CHARACTERISTICS (5 V GRAPHS)

SMALL SIGNAL UNITY GAIN FREQUENCY RESPONSE

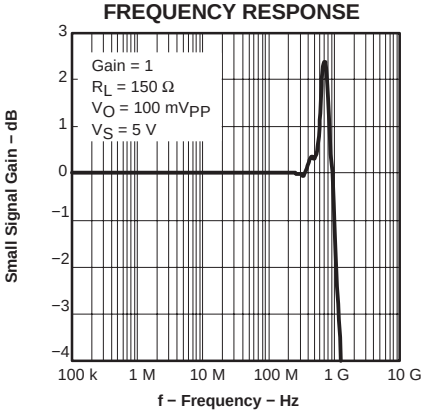


Figure 40

SMALL SIGNAL FREQUENCY RESPONSE

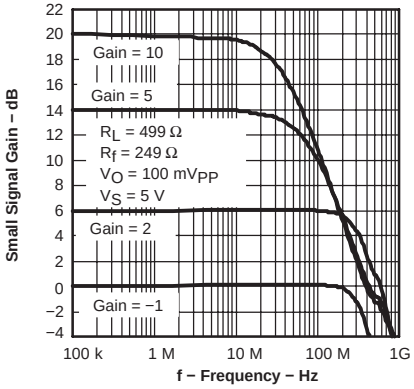


Figure 41

0.1 dB GAIN FLATNESS FREQUENCY RESPONSE

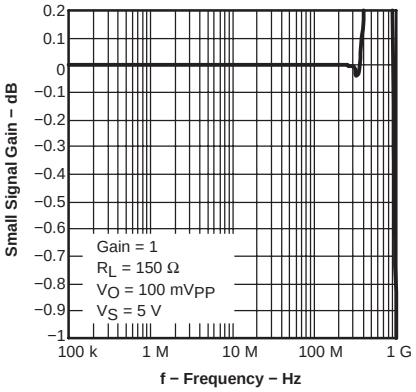


Figure 42

LARGE SIGNAL FREQUENCY RESPONSE

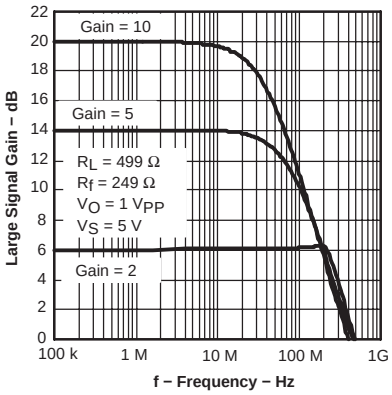


Figure 43

SLEW RATE vs OUTPUT VOLTAGE

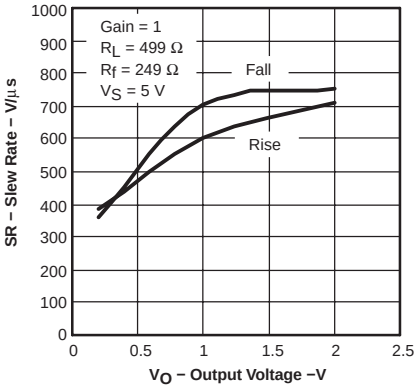


Figure 44

HARMONIC DISTORTION vs FREQUENCY

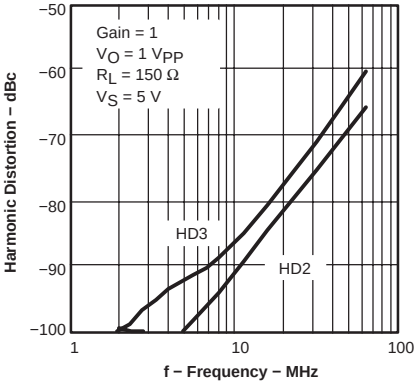


Figure 45

HARMONIC DISTORTION vs FREQUENCY

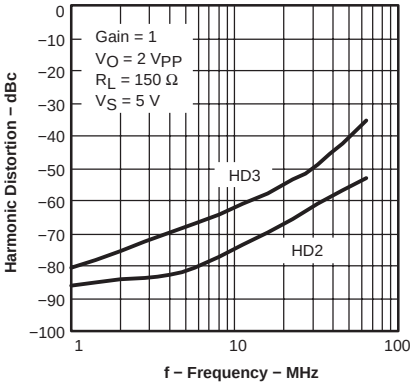


Figure 46

HARMONIC DISTORTION vs FREQUENCY

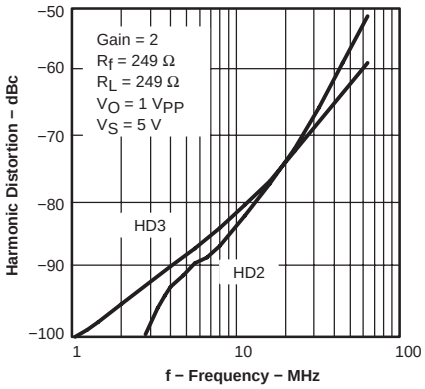


Figure 47

HARMONIC DISTORTION vs FREQUENCY

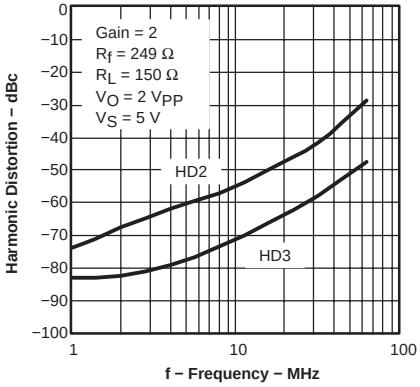


Figure 48

TYPICAL CHARACTERISTICS (5 V GRAPHS)

HARMONIC DISTORTION
vs
OUTPUT VOLTAGE SWING

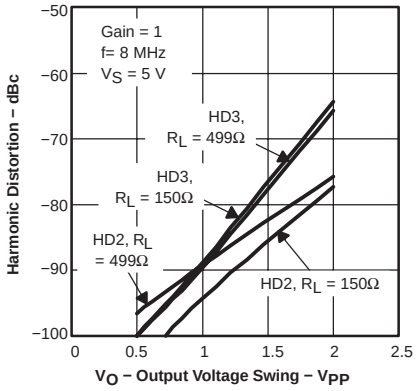


Figure 49

HARMONIC DISTORTION
vs
OUTPUT VOLTAGE SWING

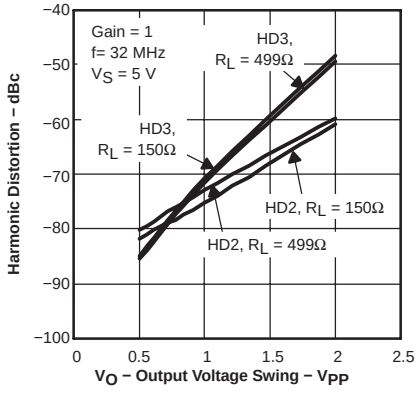


Figure 50

HARMONIC DISTORTION
vs
OUTPUT VOLTAGE SWING

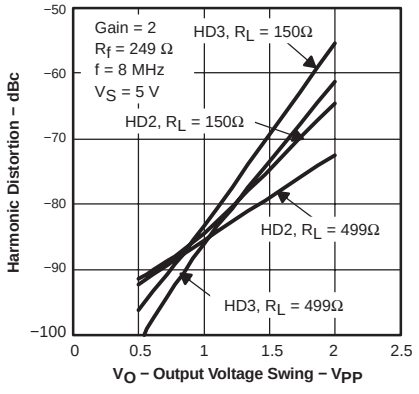


Figure 51

HARMONIC DISTORTION
vs
OUTPUT VOLTAGE SWING

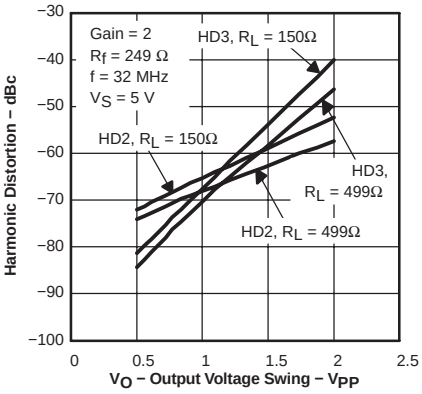


Figure 52

THIRD ORDER INTERMODULATION DISTORTION
vs
FREQUENCY

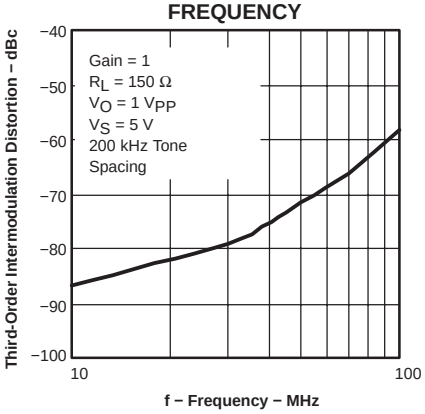


Figure 53

THIRD ORDER OUTPUT INTERCEPT POINT
vs
FREQUENCY

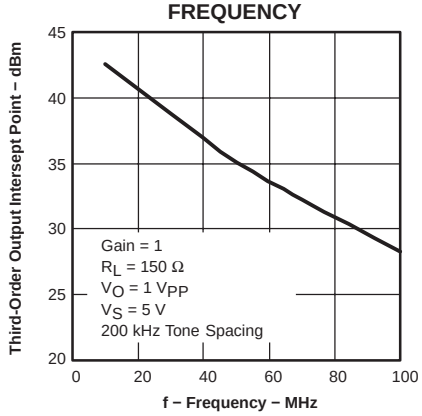


Figure 54

THIRD ORDER INTERMODULATION DISTORTION
vs
FREQUENCY

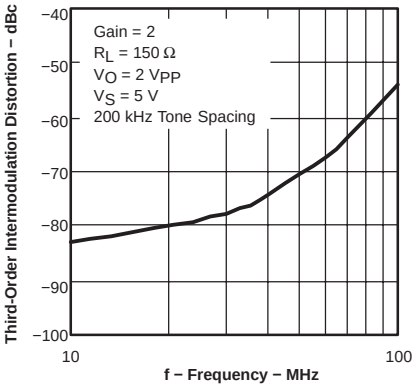


Figure 55

THIRD ORDER OUTPUT INTERCEPT POINT
vs
FREQUENCY

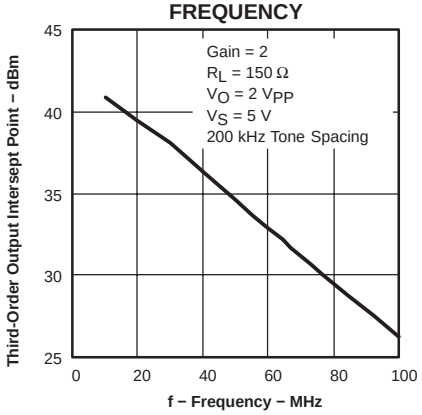


Figure 56

VOLTAGE AND CURRENT NOISE
vs
FREQUENCY

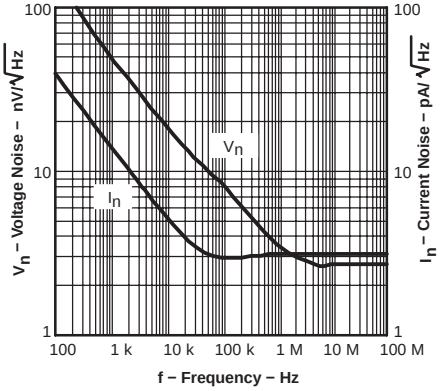


Figure 57

TYPICAL CHARACTERISTICS (5 V GRAPHS) (CONTINUED)

SETTLING TIME

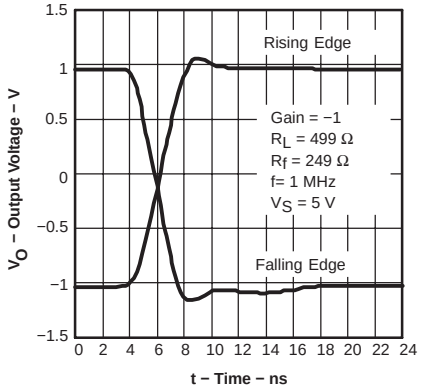


Figure 58

QUIESCENT CURRENT vs SUPPLY VOLTAGE

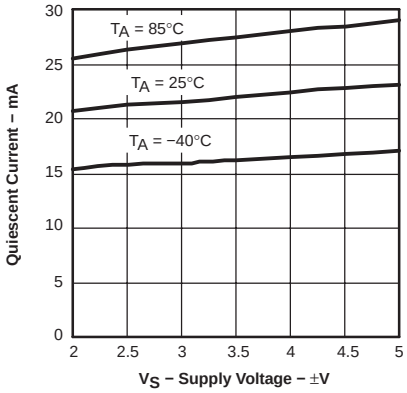


Figure 59

OUTPUT VOLTAGE vs LOAD RESISTANCE

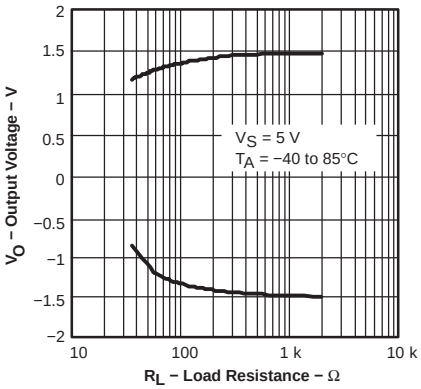


Figure 60

FREQUENCY RESPONSE vs CAPACITIVE LOAD

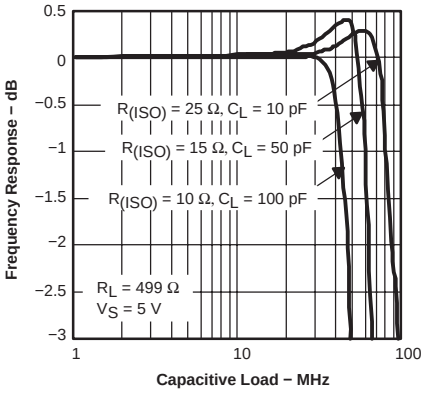


Figure 61

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

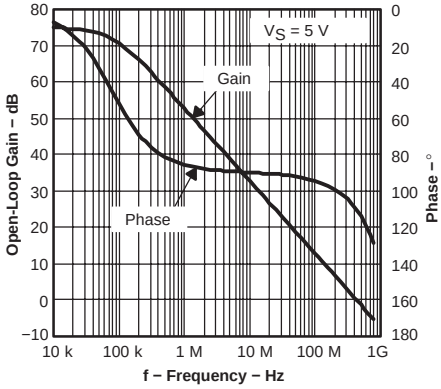


Figure 62

OPEN-LOOP GAIN vs CASE TEMPERATURE

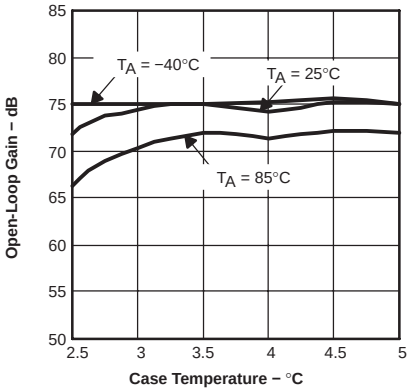


Figure 63

REJECTION RATIOS vs FREQUENCY

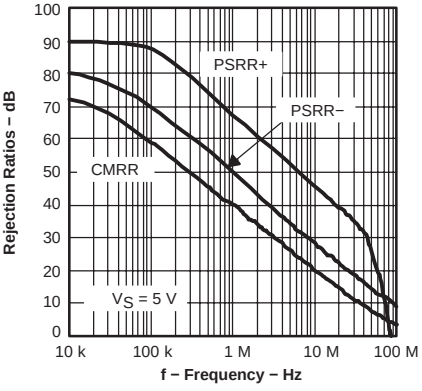


Figure 64

REJECTION RATIOS vs CASE TEMPERATURE

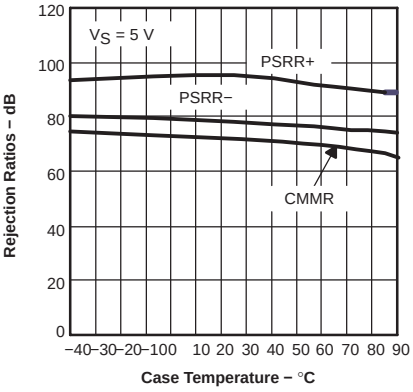


Figure 65

COMMON-MODE REJECTION RATIO vs INPUT COMMON-MODE RANGE

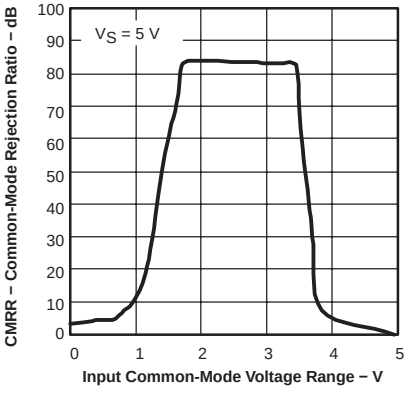


Figure 66

TYPICAL CHARACTERISTICS (5 V GRAPHS) (CONTINUED)

INPUT OFFSET VOLTAGE vs CASE TEMPERATURE

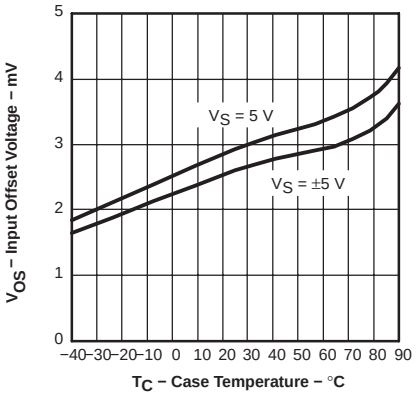


Figure 67

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

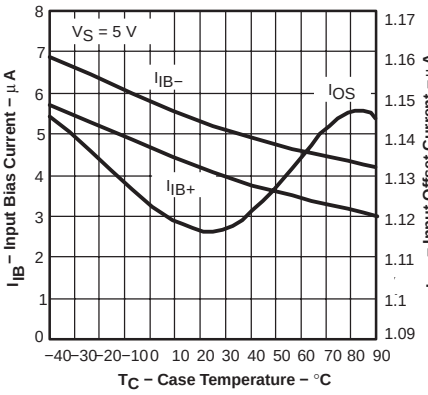


Figure 68

SMALL SIGNAL TRANSIENT RESPONSE

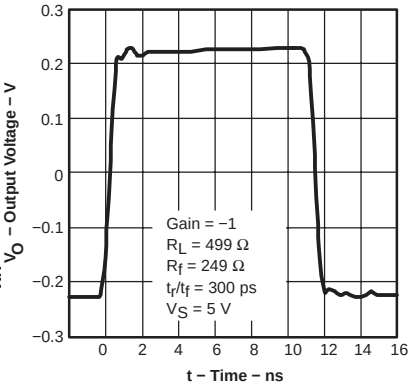


Figure 69

LARGE SIGNAL TRANSIENT RESPONSE

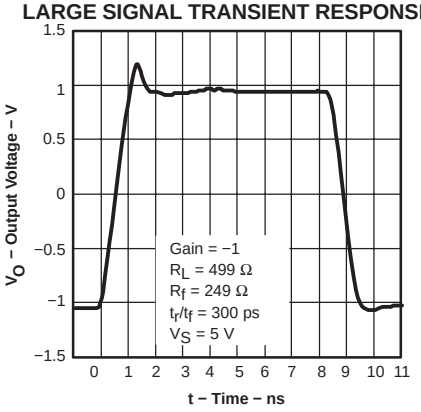


Figure 70

OVERDRIVE RECOVERY

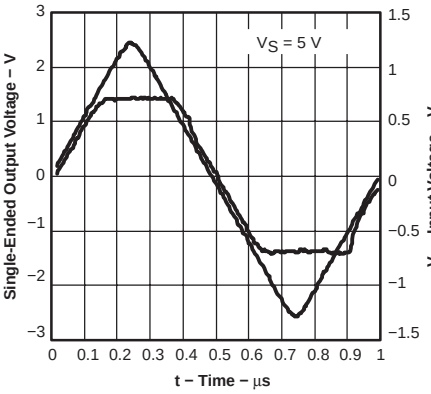


Figure 71

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

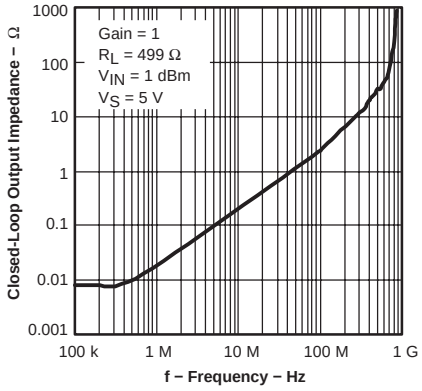


Figure 72

POWER-DOWN QUIESCENT CURRENT vs SUPPLY VOLTAGE

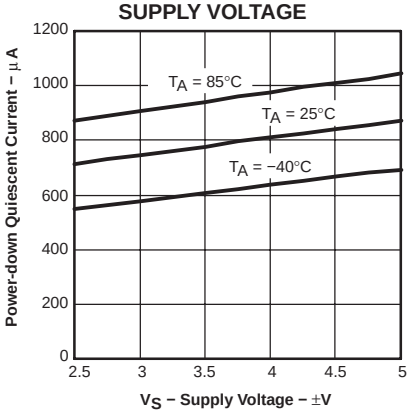


Figure 73

POWER-DOWN OUTPUT IMPEDANCE vs FREQUENCY

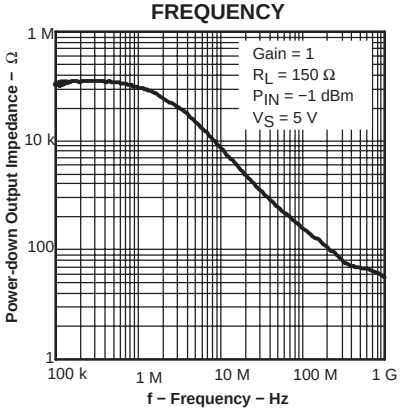


Figure 74

TURNON AND TURNOFF TIMES DELAY TIME

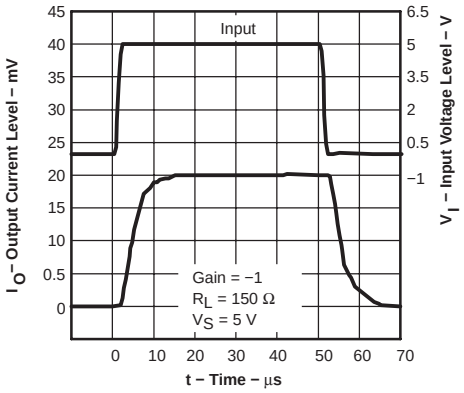


Figure 75

APPLICATION INFORMATION

HIGH-SPEED OPERATIONAL AMPLIFIERS

The THS4271 and the THS4275 operational amplifiers set new performance levels, combining low distortion, high slew rates, low noise, and a unity-gain bandwidth in excess of 1 GHz. To achieve the full performance of the amplifier, careful attention must be paid to printed-circuit board layout and component selection.

The THS4275 provides a power-down mode, providing the ability to save power when the amplifier is inactive. A reference pin is provided to allow the user the flexibility to control the threshold levels of the power-down control pin.

Applications Section Contents

WIDEBAND, NONINVERTING OPERATION

The THS4271 and the THS4275 are unity gain stable 1.4-GHz voltage feedback operational amplifiers, with and without power-down capability, designed to operate from a single 5-V to 15-V power supply.

Figure 76 is the noninverting gain configuration of 2 V/V used to demonstrate the typical performance curves. Most of the curves were characterized using signal sources with 50-Ω source impedance, and with measurement equipment presenting a 50-Ω load impedance. In Figure 76, the 49.9-Ω shunt resistor at the V_{IN} terminal matches the source impedance of the test generator. The total 499-Ω load at the output, combined with the 498-Ω total feedback network load, presents the THS4271 and THS4275 with an effective output load of 249 Ω for the circuit of Figure 76.

Voltage feedback amplifiers, unlike current feedback designs, can use a wide range of resistors values to set their gain with minimal impact on their stability and frequency response. Larger-valued resistors decrease the loading effect of the feedback network on the output of the amplifier, but this enhancement comes at the expense of additional noise and potentially lower bandwidth. Feedback resistor values between 249 Ω and 1 kΩ are recommended for most situations.

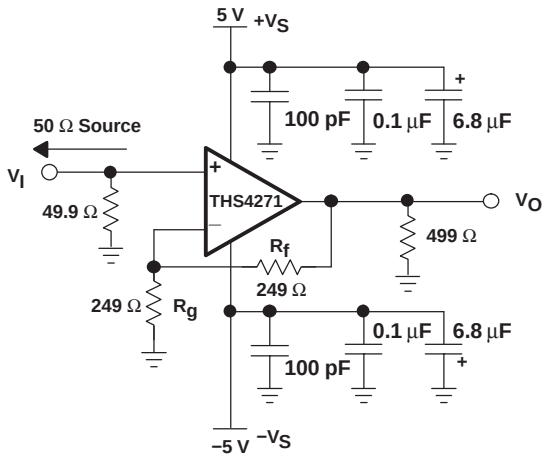


Figure 76. Wideband, Noninverting Gain Configuration

WIDEBAND, INVERTING GAIN OPERATION

Since the THS4271 and THS4275 are general-purpose, wideband voltage-feedback amplifiers, several familiar operational amplifier applications circuits are available to the designer. Figure 77 shows a typical inverting configuration where the input and output impedances and noise gain from Figure 76 are retained in an inverting circuit configuration. Inverting operation is one of the more common requirements and offers several performance benefits. The inverting configuration shows improved slew rates and distortion due to the pseudo-static voltage maintained on the inverting input.

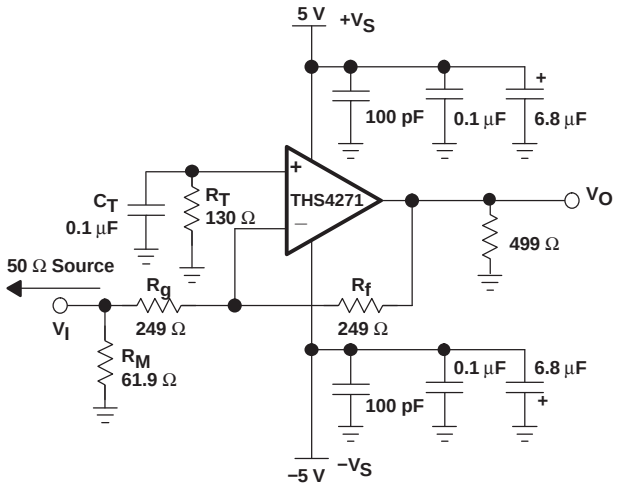


Figure 77. Wideband, Inverting Gain Configuration

In the inverting configuration, some key design considerations must be noted. One is that the gain resistor (R_g) becomes part of the signal channel input impedance. If the input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PC board trace, or other transmission line conductors), R_g may be set equal to the required termination value and R_f adjusted to give the desired gain. However, care must be taken when dealing with low inverting gains, as the resultant feedback resistor value can present a significant load to the amplifier output. For an inverting gain of 2, setting R_g to 49.9 Ω for input matching eliminates the need for R_M but requires a 100-Ω feedback resistor. This has an advantage of the noise gain becoming equal to 2 for a 50-Ω source impedance—the same as the noninverting circuit in Figure 76. However, the amplifier output now sees the 100-Ω feedback resistor in parallel with the external load. To eliminate this excessive loading, it is preferable to increase both R_g and R_f, values, as shown in Figure 77, and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_g and R_M.

The next major consideration is that the signal source impedance becomes part of the noise gain equation and hence influences the bandwidth. For example, the R_M value combines in parallel with the external 50-Ω source impedance (at high frequencies), yielding an effective source impedance of 50 Ω || 61.9 Ω = 27.7 Ω. This impedance is then added in series with R_g for calculating the noise gain. The result is 1.9 for Figure 77, as opposed to the 1.8 if R_M is eliminated. The bandwidth is lower for the gain of –2 circuit, Figure 77, (NG=+1.9) than for the gain of +2 circuit in Figure 76.

The last major consideration in inverting amplifier design is setting the bias current cancellation resistor on the noninverting input. If the resistance is set equal to the total dc resistance looking out of the inverting terminal, the output dc error, due to the input bias currents, is reduced to (input offset current) multiplied by R_f in Figure 77, the dc-source impedance looking out of the inverting terminal is 249 Ω || (249 Ω + 27.7 Ω) = 130 Ω. To reduce the additional high-frequency noise introduced by the resistor at the noninverting input, and power-supply feedback, R_T is bypassed with a capacitor to ground.

SINGLE SUPPLY OPERATION

The THS4271 is designed to operate from a single 5-V to 15-V power supply. When operating from a single power supply, care must be taken to ensure the input signal and amplifier are biased appropriately to allow for the maximum output voltage swing. The circuits shown in Figure 78 demonstrate methods to configure an amplifier in a manner conducive for single supply operation.

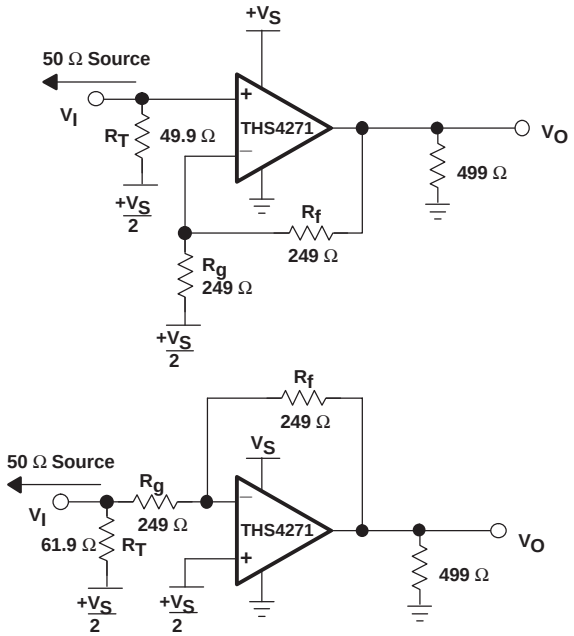


Figure 78. DC-Coupled Single Supply Operation

Saving Power With Power-Down Functionality and Setting Threshold Levels With the Reference Pin

The THS4275 features a power-down pin ($\overline{PD}$) which lowers the quiescent current from 22 mA down to 700 μA, ideal for reducing system power.

The power-down pin of the amplifiers defaults to the positive supply voltage in the absence of an applied voltage, putting the amplifier in the power-on mode of operation. To turn off the amplifier in an effort to conserve power, the power-down pin can be driven towards the

negative rail. The threshold voltages for power-on and power-down are relative to the supply rails and given in the specification tables. Above the *Enable Threshold Voltage*, the device is on. Below the *Disable Threshold Voltage*, the device is off. Behavior in between these threshold voltages is not specified.

Note that this power-down functionality is just that; the amplifier consumes less power in power-down mode. The power-down mode is not intended to provide a high-impedance output. In other words, the power-down functionality is not intended to allow use as a 3-state bus driver. When in power-down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain setting resistors, but the output impedance of the device itself varies depending on the voltage applied to the outputs.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach 50% of the nominal quiescent current. The time delays are on the order of microseconds because the amplifier moves in and out of the linear mode of operation in these transitions.

Power-Down Reference Pin Operation

In addition to the power-down pin, the THS4275 also features a reference pin (REF) which allows the user to control the enable or disable power-down voltage levels applied to the $\overline{PD}$ pin. Operation of the reference pin as it relates to the power-down pin is described below.

In most split-supply applications, the reference pin is connected to ground. In some cases, the user may want to connect it to the negative or positive supply rail. In either case, the user needs to be aware of the voltage level thresholds that apply to the power-down pin. The tables below show examples and illustrate the relationship between the reference voltage and the power-down thresholds.

POWER-DOWN THRESHOLD VOLTAGE LEVELS (REF ≤ MIDRAIL)			
SUPPLY VOLTAGE(V)	**REFERENCE PIN VOLTAGE (V)**	**ENABLE LEVEL (V)**	**DISABLE LEVEL (V)**
±5	GND	≥ 1.8	≤ 1
	−2.5	≥ −0.7	≤ −1.5
	−5	≥ −3.2	≤ −4
5	GND	≥ 1.8	≤ 1
	1	≥ 2.8	≤ 2
	2.5	≥ 4.3	≤ 3.5

In the above table, the threshold levels are derived by the following equations:

REF + 1.8 V for enable
REF + 1 V for disable

Note that in order to maintain these threshold levels, the reference pin can be any voltage between Vs− or GND up to Vs/2 (midrail).

POWER-DOWN THRESHOLD VOLTAGE LEVELS (REF > MIDRAIL)			
SUPPLY VOLTAGE (V)	**REFERENCE PIN VOLTAGE (V)**	**ENABLE LEVEL (V)**	**DISABLE LEVEL (V)**
±5	Floating or 5	≥ 4	≤ 3.3
	2.5	≥ 1.5	≤ 0.8
	1	≥ 0	≤ −0.7
5	Floating or 5	≥ 3.3	≤ 3.3
	4	≥ 3	≤ 2.3
	3.5	≥ 2.5	≤ 1.8

In the above table, the threshold levels are derived by the following equations:

REF − 1 V for enable
REF − 1.7 V for disable

Note that in order to maintain these threshold levels, the reference pin can be any voltage between (Vs+/2) + 1 V to Vs+.

The recommended mode of operation is to tie the reference pin to midrail, thus setting the threshold levels to midrail +1 V and midrail +1.8 V.

NO. OF CHANNELS	PACKAGES
Single (8 pin)	THS4275D, THS4275DGN, and THS4275DRB

Power Supply Decoupling Techniques and Recommendations

Power supply decoupling is a critical aspect of any high-performance amplifier design process. Careful decoupling provides higher quality ac performance (most notably improved distortion performance). The following guidelines ensure the highest level of performance.

1. Place decoupling capacitors as close to the power supply inputs as possible, with the goal of minimizing the inductance of the path from ground to the power supply.
2. Placement priority should put the smallest valued capacitors closest to the device.
3. Use of solid power and ground planes is recommended to reduce the inductance along power supply return current paths, with the exception of the areas underneath the input and output pins.
4. Recommended values for power supply decoupling include a bulk decoupling capacitor (6.8 to 22 μF), a mid-range decoupling capacitor (0.1 μF) and a high frequency decoupling capacitor (1000 pF) for each supply. A 100-pF capacitor can be used across the supplies as well for extremely high frequency return currents, but often is not required.

APPLICATION CIRCUITS

Driving an Analog-to-Digital Converter With the THS4271

The THS4271 can be used to drive high-performance analog-to-digital converters. Two example circuits are presented below.

The first circuit uses a wideband transformer to convert a single-ended input signal into a differential signal. The differential signal is then amplified and filtered by two THS4271 amplifiers. This circuit provides low intermodulation distortion, suppressed even-order distortion, 14 dB of voltage gain, a 50-Ω input impedance, and a single-pole filter at 100 MHz. For applications without signal content at dc, this method of driving ADCs can be useful. Where dc information content is required, the THS4500 family of fully differential amplifiers may be applicable.

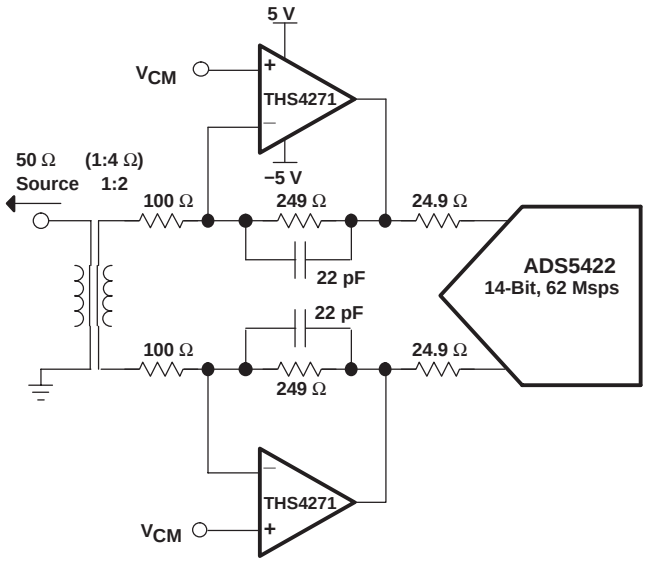
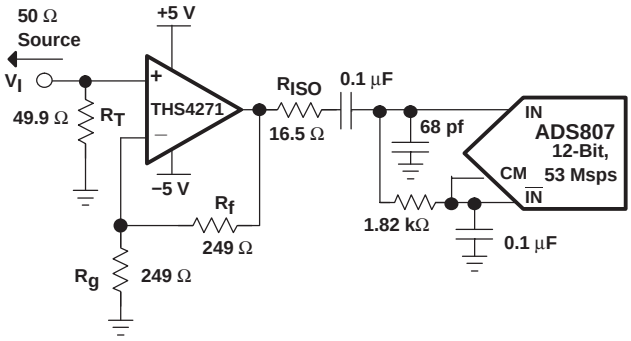


Figure 79. A Linear, Low Noise, High Gain ADC Preamplifier

The second circuit depicts single-ended ADC drive. While not recommended for optimum performance using converters with differential inputs, satisfactory performance can sometimes be achieved with single-ended input drive. An example circuit is shown here for reference.



NOTE: For the best performance, high-speed ADCs should be driven differentially. See the THS4500 family of devices for more information.

Figure 80. Driving an ADC With a Single-Ended Input

Using the THS4271 as a DAC Output Buffer

Two example circuits are presented here showing the THS4271 buffering the output of a digital-to-analog converter. The first circuit performs a differential to single-ended conversion with the THS4271 configured as a difference amplifier. The difference amplifier can double as the termination mechanism for the DAC outputs as well.

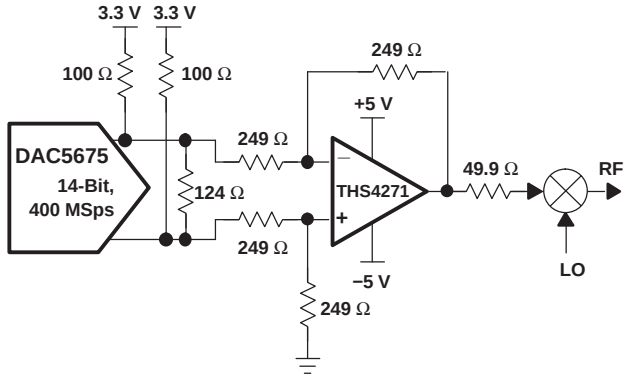


Figure 81. Differential to Single-Ended Conversion of a High-Speed DAC Output

For cases where a differential signaling path is desirable, a pair of THS4271 amplifiers can be used as output buffers. The circuit depicts differential drive into a mixer's IF inputs, coupled with additional signal gain and filtering.

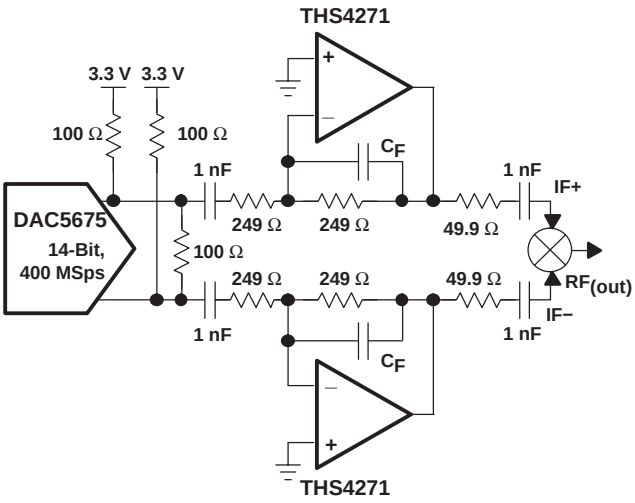


Figure 82. Differential Mixer Drive Circuit Using the DAC5675 and the THS4271

Active Filtering With the THS4271

High-frequency active filtering with the THS4271 is achievable due to the amplifier's high slew-rate, wide bandwidth, and voltage feedback architecture. Several options are available for high-pass, low-pass, bandpass, and bandstop filters of varying orders. A simple two-pole low pass filter is presented here as an example, with two poles at 100 MHz.

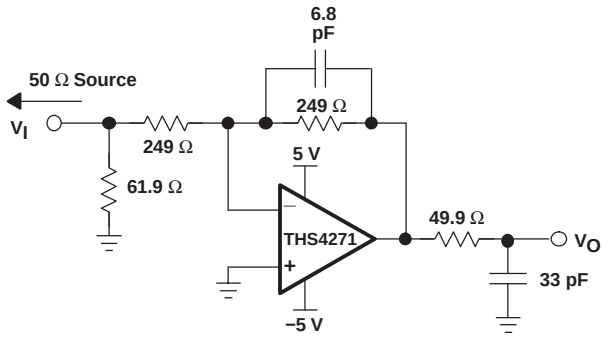


Figure 83. A Two-Pole Active Filter With Two Poles Between 90 MHz and 100 MHz

A Low-Noise Receiver With the THS4271

A combination of two THS4271 amplifiers can create a high-speed, low-distortion, low-noise differential receiver circuit as depicted in Figure 84. With both amplifiers operating in the noninverting mode of operation, the circuit presents a high load impedance to the source. The designer has the option of controlling the impedance through termination resistors if a matched termination impedance is desired.

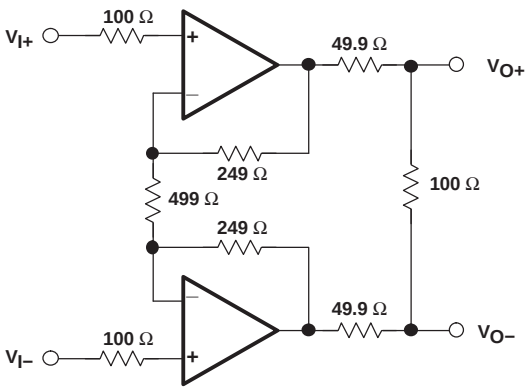


Figure 84. A High Input Impedance, Low Noise, Differential Receiver

A modification on this circuit to include a difference amplifier turns this circuit into a high-speed instrumentation amplifier, as shown in Figure 85.

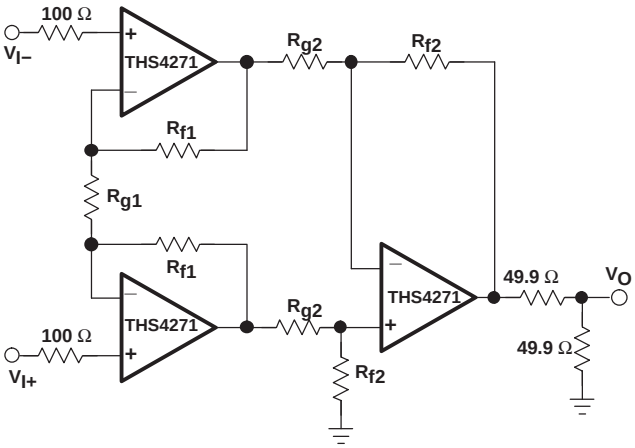


Figure 85. A High-Speed Instrumentation Amplifier

$$V_O = \frac{1}{2}\left(1 + \frac{2R_{f1}}{R_{g1}}\right)(V_{i+} - V_{i-})\left(\frac{R_{f2}}{R_{g2}}\right) \quad (1)$$

THEORY AND GUIDELINES

Distortion Performance

The THS4271 provides excellent distortion performance into a 150-Ω load. Relative to alternative solutions, it provides exceptional performance into lighter loads, as well as exceptional performance on a single 5-V supply. Generally, until the fundamental signal reaches high frequency or power levels, the 2nd harmonic dominates the total harmonic distortion with a negligible 3rd harmonic component. Focusing then on the 2nd harmonic, increasing the load impedance improves distortion

directly. The total load includes the feedback network; in the noninverting configuration (see Figure 76) this is the sum of R_f and R_g, while in the inverting configuration (see Figure 77), only R_f needs to be included in parallel with the actual load.

LINEARITY: DEFINITIONS, TERMINOLOGY, CIRCUIT TECHNIQUES, AND DESIGN TRADEOFFS

The THS4271 features excellent distortion performance for monolithic operational amplifiers. This section focuses on the fundamentals of distortion, circuit techniques for reducing nonlinearity, and methods for equating distortion of operational amplifiers to desired linearity specifications in RF receiver chains.

Amplifiers are generally thought of as *linear* devices. The output of an amplifier is a linearly scaled version of the input signal applied to it. However, amplifier transfer functions are nonlinear. Minimizing amplifier nonlinearity is a primary design goal in many applications.

Intercept points are specifications long used as key design criteria in the RF communications world as a metric for the intermodulation distortion performance of a device in the signal chain (e.g., amplifiers, mixers, etc.). Use of the intercept point, rather than strictly the intermodulation distortion, allows simpler system-level calculations. Intercept points, like noise figures, can be easily cascaded back and forth through a signal chain to determine the overall receiver chain's intermodulation distortion performance. The relationship between intermodulation distortion and intercept point is depicted in Figure 86 and Figure 87.

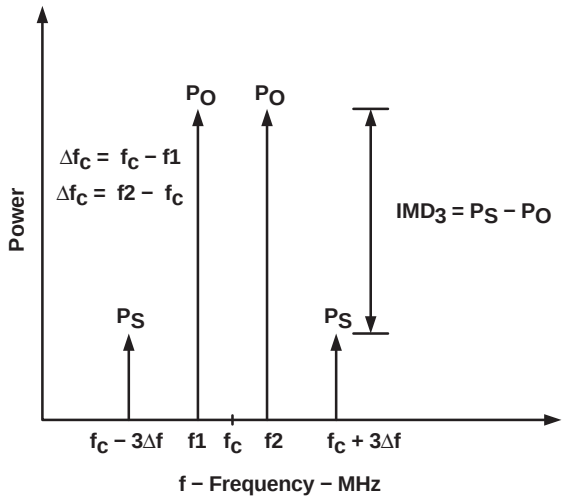


Figure 86

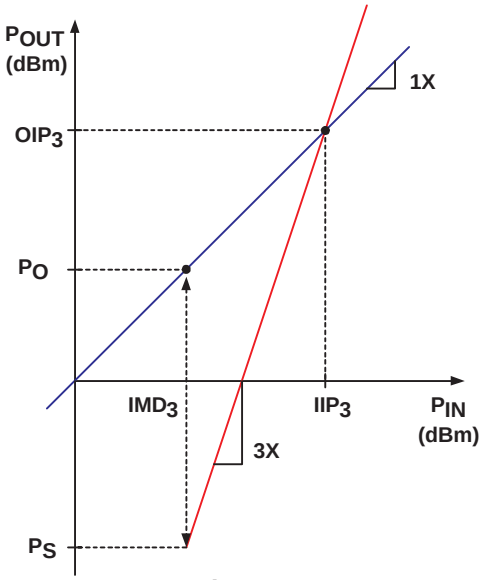


Figure 87

Due to the intercept point's ease of use in system level calculations for receiver chains, it has become the specification of choice for guiding distortion-related design decisions. Traditionally, these systems use primarily class-A, single-ended RF amplifiers as gain blocks. These RF amplifiers are typically designed to operate in a 50-Ω environment. Giving intercept points in dBm, implies an associated impedance (50 Ω).

However, with an operational amplifier, the output does not require termination as an RF amplifier would. Because closed-loop amplifiers deliver signals to their outputs regardless of the impedance present, it is important to comprehend this when evaluating the intercept point of an operational amplifier. The THS4271 yields optimum distortion performance when loaded with 150 Ω to 1 kΩ, which is similar to the input impedance of an analog-to-digital converter over its input frequency band.

As a result, terminating the input of the ADC to 50 Ω can actually be detrimental to systems performance.

The discontinuity between open-loop, class-A amplifiers and closed-loop, class-AB amplifiers becomes apparent when comparing the intercept points of the two types of devices. Equations 1 and 2 gives the definition of an intercept point, relative to the intermodulation distortion.

$$OIP_3 = P_O + \left(\frac{|IMD_3|}{2}\right) \text{ where} \quad (2)$$

$$P_O = 10 \log\left(\frac{V_P^2}{2R_L \times 0.001}\right) \quad (3)$$

NOTE: P_O is the output power of a single tone, R_L is the load resistance, and V_P is the peak voltage for a single tone.

NOISE ANALYSIS

High slew rate, unity gain stable, voltage-feedback operational amplifiers usually achieve their slew rate at the expense of a higher input noise voltage. The 3-nV/√Hz input voltage noise for the THS4271 and THS4275 is, however, much lower than comparable amplifiers. The input-referred voltage noise, and the two input-referred current noise terms (3 pA/√Hz), combine to give low output noise under a wide variety of operating conditions. Figure 88 shows the amplifier noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

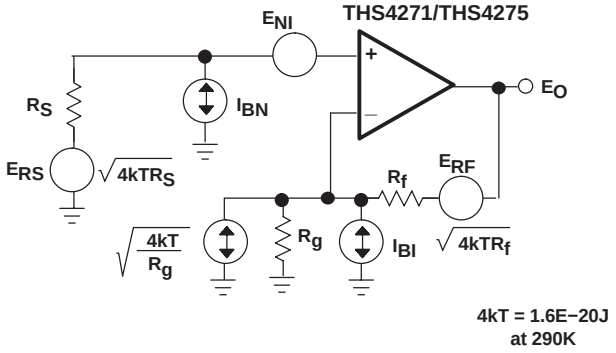


Figure 88. Noise Analysis Model

The total output shot noise voltage can be computed as the square of all square output noise voltage contributors. Equation 3 shows the general form for the output noise voltage using the terms shown in Figure 88:

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_f\right)^2 + 4kTR_fNG} \quad (4)$$

Dividing this expression by the noise gain (NG=(1+ R_f/R_g)) gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 4:

$$E_O = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_f}{NG}\right)^2 + \frac{4kTR_f}{NG}} \quad (5)$$

Evaluation of these two equations for the circuit and component values shown in Figure 76 gives a total output spot noise voltage of 12.2 nV/√Hz and a total equivalent input spot noise voltage of 6.2 nV/√Hz. This includes the noise added by the resistors. This total input-referred spot noise voltage is not much higher than the 3 nV/√Hz specification for the amplifier voltage noise alone.

Driving Capacitive Loads

One of the most demanding, and yet common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter, including additional external capacitance, which may be recommended to improve A/D linearity. A high-speed, high open-loop gain amplifier like the THS4271 can be susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. When the primary considerations are frequency response flatness, pulse response fidelity, or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The *Typical Characteristics* show the recommended isolation resistor vs capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2 pF can begin to degrade the performance of the THS4271. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the THS4271 output pin (see Board Layout Guidelines).

The criterion for setting this $R_{(ISO)}$ resistor is a maximum bandwidth, flat frequency response at the load. For a gain of +2, the frequency response at the output pin is already slightly peaked without the capacitive load, requiring relatively high values of $R_{(ISO)}$ to flatten the response at the load. Increasing the noise gain also reduces the peaking.

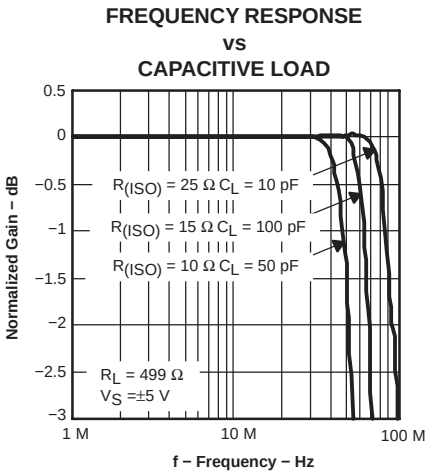


Figure 89. Isolation Resistor Diagram

BOARD LAYOUT

Achieving optimum performance with a high frequency amplifier like the THS4271 requires careful attention to board layout parasitics and external component types.

Recommendations that optimize performance include:

1. **Minimize parasitic capacitance to any ac ground for all of the signal I/O pins.** Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

2. **Minimize the distance (< 0.25") from the power supply pins to high frequency 0.1-μF decoupling capacitors.** At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (2.2 μF to 6.8 μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

3. **Careful selection and placement of external components preserves the high frequency performance of the THS4271.** Resistors should be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wire-wound type resistors in a high frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input-termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 2 kΩ, this parasitic capacitance can add a pole and/or a zero below 400 MHz that can effect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations. A good starting point for design is to set the R_f to 249 Ω for low-gain, noninverting applications. Doing this automatically keeps the resistor noise terms low and minimizes the effect of their parasitic capacitance.

4. **Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines.** For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic capacitive loads (<4 pF) may not need an $R_{(ISO)}$, since the THS4271 is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an $R_{(ISO)}$ are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary onboard, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS4271 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the

parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of $R_{(ISO)}$ vs capacitive load. This does not preserve signal integrity or a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

5. **Socketing a high speed part like the THS4271 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create a troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. The best results are obtained by soldering the THS4271 onto the board.

PowerPAD™ DESIGN CONSIDERATIONS

The THS4271 and THS4275 are available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 90(a) and Figure 90(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 90(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows both assembly and thermal management in one manufacturing operation.

During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the heretofore awkward mechanical methods of heatsinking.

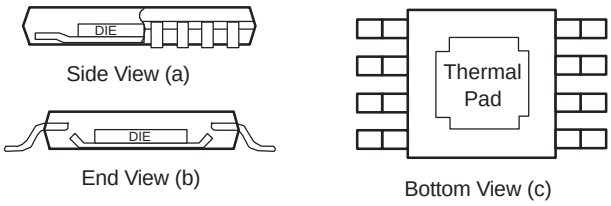


Figure 90. Views of Thermally Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

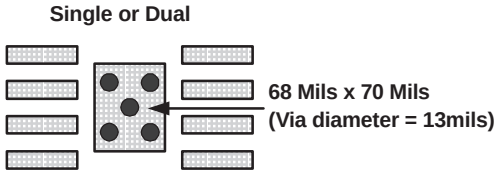


Figure 91. PowerPAD PCB Etch and Via Pattern

PowerPAD PCB LAYOUT CONSIDERATIONS

1. Prepare the PCB with a top side etch pattern as shown in Figure 91. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. The holes should be 13 mils in diameter. Keep the holes small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. They help dissipate the heat generated by the THS4271 and THS4275 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This resistance makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS4271 and THS4275 PowerPAD package should make their connection to the internal ground plane, with a complete connection around the entire circumference of the plated-through hole.

6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.

7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.

8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For a given θ_{JA} , the maximum power dissipation is shown in Figure 92 and is calculated by the equation 5:

$$P_D = \frac{T_{max} - T_A}{\theta_{JA}} \quad (6)$$

where:
P_D = Maximum power dissipation of THS4271 (W)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to the case
θ_{CA} = Thermal coefficient from the case to ambient air (°C/W).

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (Class AB), most of the heat dissipation is at low output voltages with high output currents.

The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. For a single package, the sum of the RMS output currents and voltages should be used to choose the proper package.

THERMAL ANALYSIS

The THS4271 device does not incorporate automatic thermal shutoff protection, so the designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of 150°C is exceeded.

The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}} \quad (7)$$

where:
P_{Dmax} is the maximum power dissipation in the amplifier (W).
T_{max} is the absolute maximum junction temperature (°C).
T_A is the ambient temperature (°C).
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

For systems where heat dissipation is more critical, the THS4271 is offered in an 8-pin MSOP with PowerPAD. The thermal coefficient for the MSOP PowerPAD package is substantially improved over the traditional SOIC. Maximum power dissipation levels are depicted in the graph for the two packages. The data for the DGN package assumes a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application notes in the *Additional Reference Material* section at the end of the data sheet.

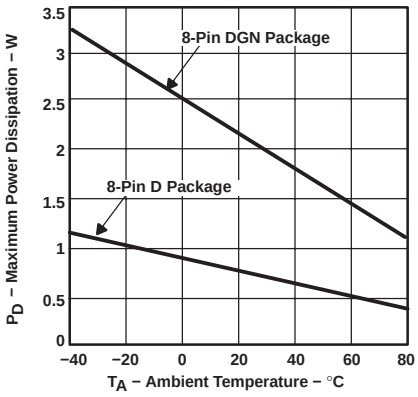


Figure 92. Maximum Power Dissipation vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to consider not only quiescent power dissipation, but also dynamic power dissipation. Often maximum power is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

DESIGN TOOLS

Performance vs Package Options

The THS4271 and THS4275 are offered in different package options. However, performance may be limited due to package parasitics and lead inductance in some packages. In order to achieve maximum performance of the THS4271 and THS4275, Texas Instruments recommends using the leadless MSOP (DRB) or MSOP (DGN) packages, in addition to proper high-speed PCB layout. Figure 93 shows the unity gain frequency response of the THS4271 using the leadless MSOP, MSOP, and SOIC package for comparison. Using the THS4271 and THS4275 in a unity gain with the SOIC package may result in the device becoming unstable. In higher gain configurations, this effect is mitigated by the reduced bandwidth. As such, the SOIC is suitable for application with gains equal to or higher than +2 V/V or (−1 V/V).

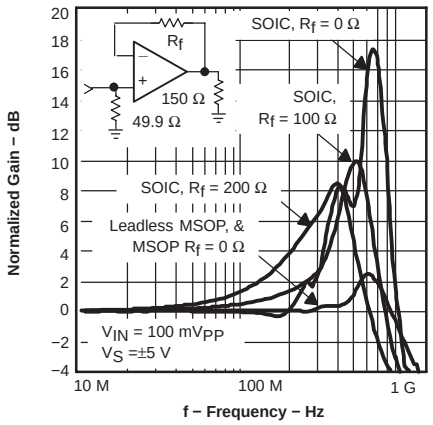


Figure 93. Effects of Unity Gain Frequency Response for Differential Packages

Evaluation Fixtures, Spice Models, and Applications Support

Texas Instruments is committed to providing its customers with the highest quality of applications support. To support this goal, evaluation boards have been developed for the THS4271 operational amplifier. Three evaluation boards are available: one THS4271 and one THS4275, both are configurable for different gains and a third for a gain of +1 (THS4271 only). These boards are easy to use, allowing for straightforward evaluation of the device. These evaluation boards can be ordered through the Texas Instruments web site, www.ti.com, or through your local Texas Instruments sales representative. Schematics for the evaluation boards are shown below.

The THS4271/THS4275 EVM board shown in Figure 97 through Figure 100 is designed to accommodate different gain configurations. Its default component values are set to give a gain of two. The EVM can be configured in a gain of +1; however, it is strongly not recommended. Evaluating the THS4271/THS4275 in a gain of one using this EVM may cause the part to become unstable. The stability of the device can be controlled by adding a large resistor in the feedback path, the performance is sacrificed. Figure 94 shows the small signal frequency response of the THS4271 with different feedback resistors in the feedback path. Figure 95 is the small frequency response of the THS4271 using the gain of 1 EVM.

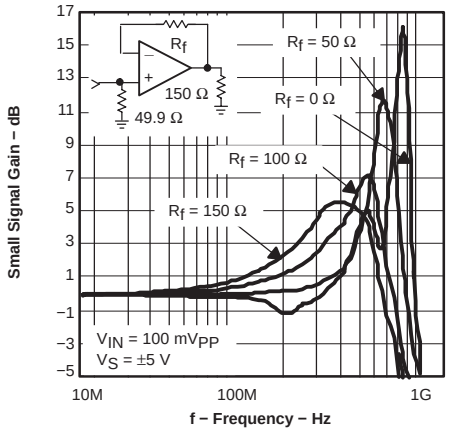


Figure 94. Frequency Response vs Feedback Resistor Using the EDGE #6439527 EVM

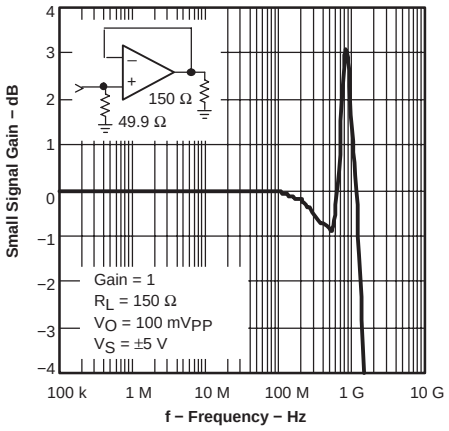


Figure 95. Frequency Response Using the EDGE # 6443547 G = +1 EVM

The peaking in the frequency response is due to the lead inductance in the feedback path. Each pad and trace on a PCB has an inductance associated with it, which in conjunction with the inductance associated with the package may cause peaking in the frequency response, causing the device to become unstable.

In order to achieve the maximum performance of the device, PCB layout is critical. Texas Instruments has developed an EVM for the evaluation of the THS4271 in a gain of one. The EVM is shown in Figure 102 through Figure 105. This EVM is designed to minimize peaking in the unity gain configuration.

Minimizing the inductance in the feedback path is critical for reducing the peaking of the frequency response in unity gain. The recommended maximum inductance allowed in the feedback path is 4 nH. This can be calculated by using Equation 8.

$$L(nH) = K\ell\left[\ln\frac{2\ell}{W+T} + 0.223\frac{W+T}{\ell} + 0.5\right] \quad (8)$$

where:
W = Width of trace in inches.
ℓ = Length of the trace in inches.
T = Thickness of the trace in inches.
K = 5.08 for dimensions in inches and K = 2 for dimensions in cm.

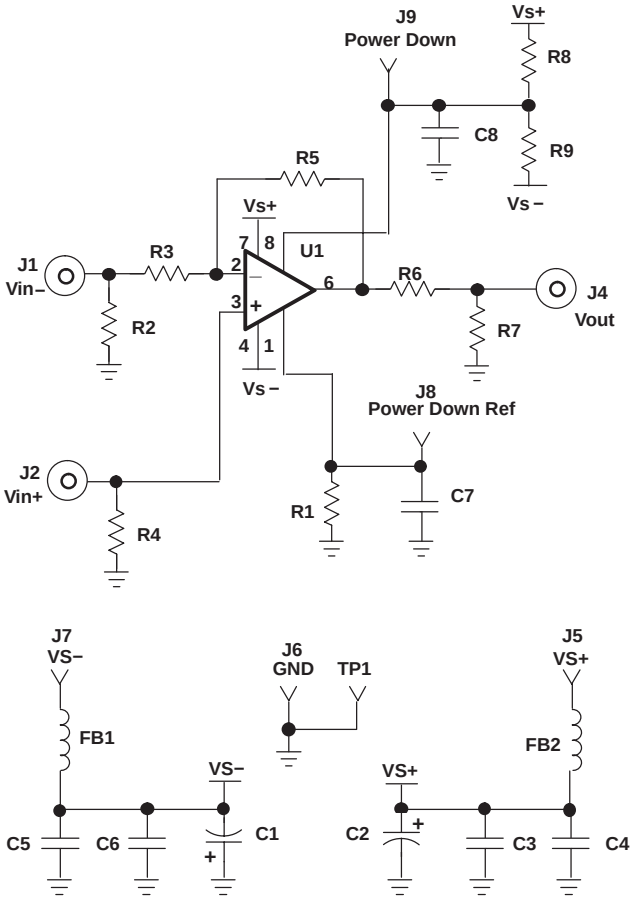


Figure 96. THS4271/THS4275 EVM Circuit Configuration

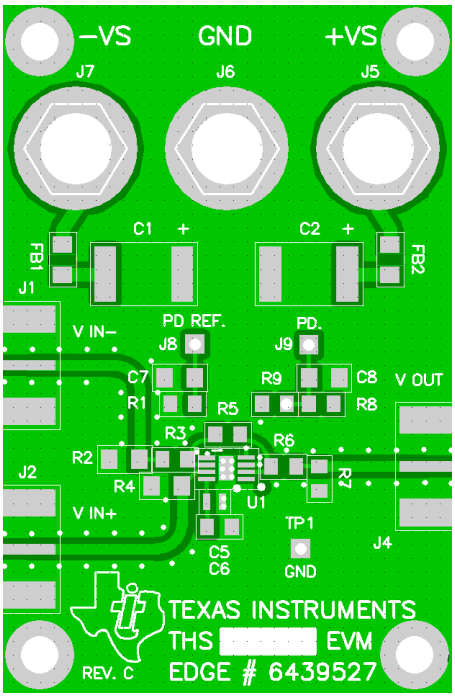


Figure 97. THS4271/THS4275 EVM Board Layout (Top Layer)

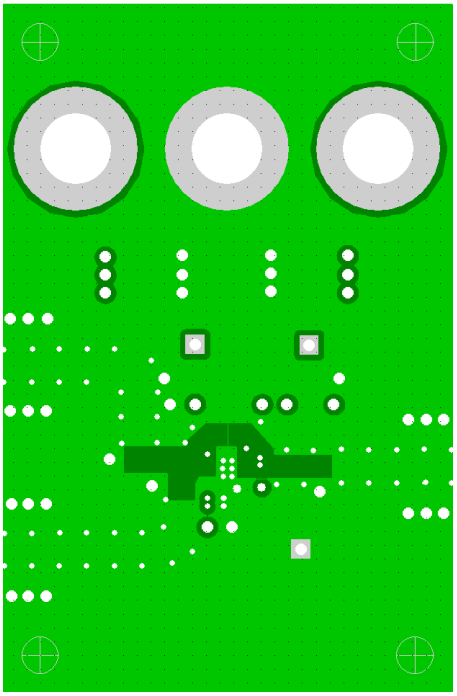


Figure 98. THS4271/THS4275 EVM Board Layout (Second Layer, Ground)

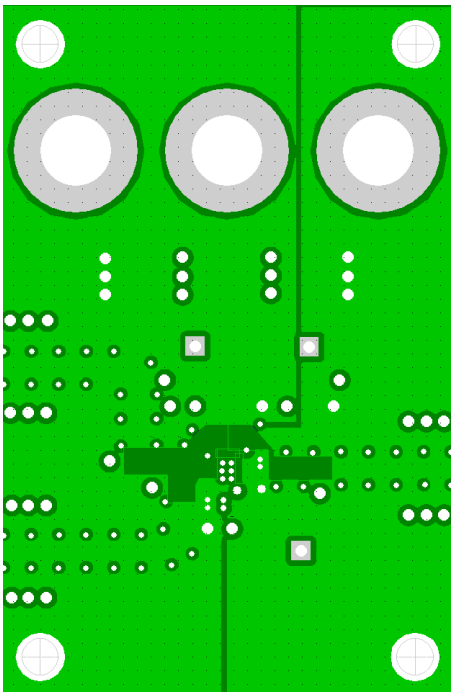


Figure 99. THS4271/THS4275 EVM Board Layout (Third Layer, Power)

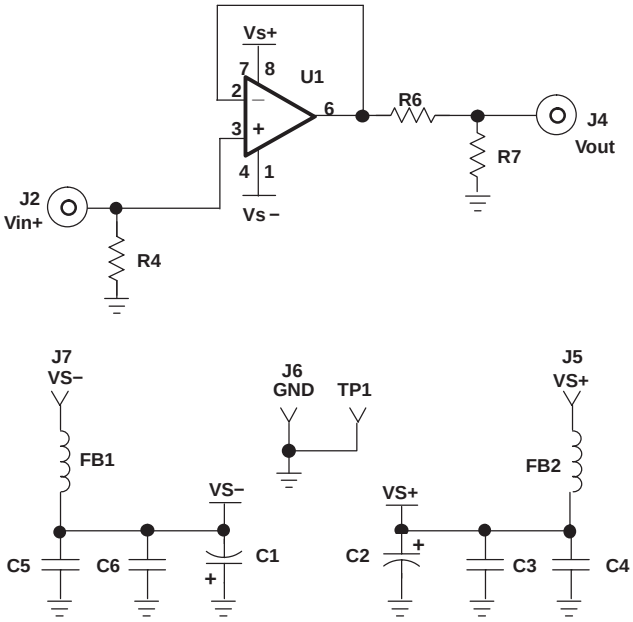


Figure 101. THS4271 Unity Gain EVM Circuit Configuration

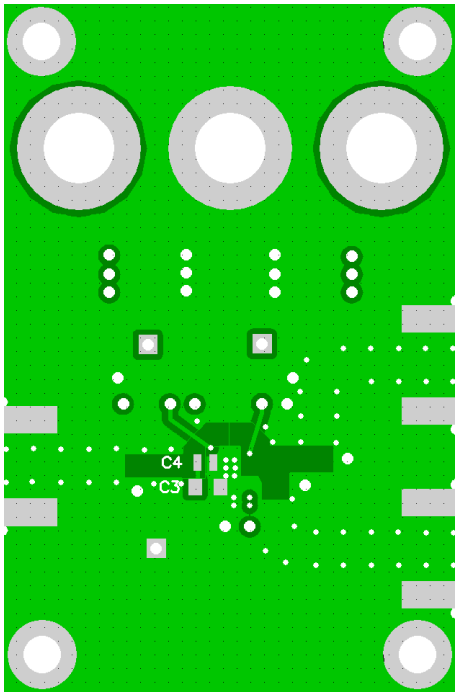


Figure 100. THS4271/THS4275 EVM Board Layout (Bottom Layer)

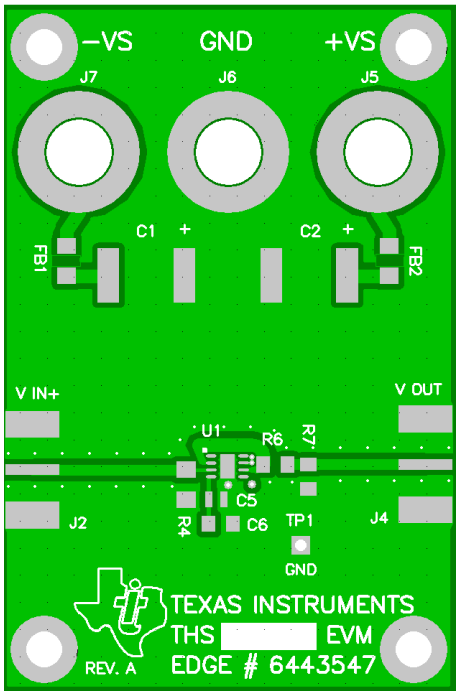


Figure 102. THS4271 Unity Gain EVM Board Layout (Top Layer)

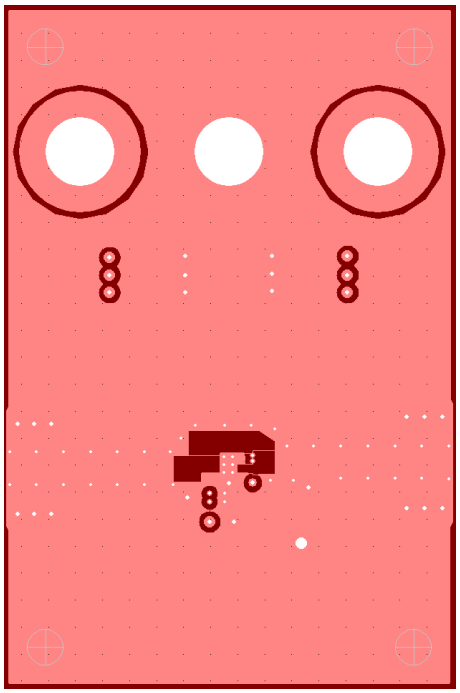


Figure 103. THS4271 Unity Gain EVM Board Layout (Second Layer, Ground)

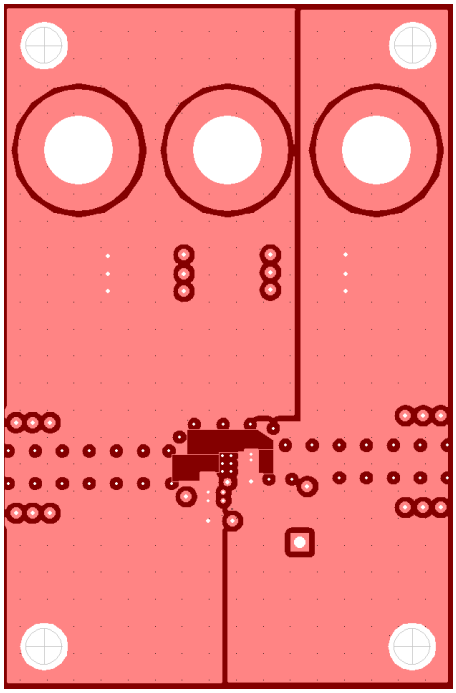


Figure 104. THS4271 Unity Gain EVM Board Layout (Third Layer, Power)

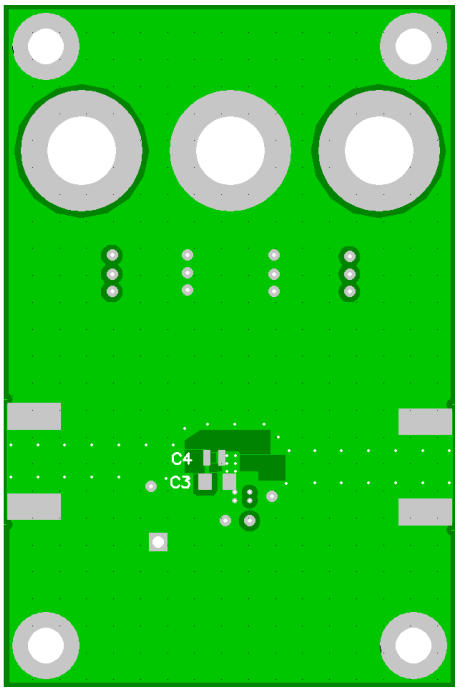


Figure 105. THS4271 Unity Gain EVM Board Layout (Bottom Layer)

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the THS4271 is available through either the Texas Instruments web site (www.ti.com) or as one model on a disk from the Texas Instruments Product Information Center (1−800−548−6132). The PIC is also available for design assistance and detailed product information at this number. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. They are not intended to model the distortion characteristics of the amplifier, nor do they attempt to distinguish between the package types in their small-signal ac performance. Detailed information about what is and is not modeled is contained in the model file itself.

ADDITIONAL REFERENCE MATERIAL

- *PowerPAD Made Easy*, application brief (SLMA004)
- *PowerPAD Thermally Enhanced Package*, technical brief (SLMA002)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
THS4271MDGNREP	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/05610-01YE	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

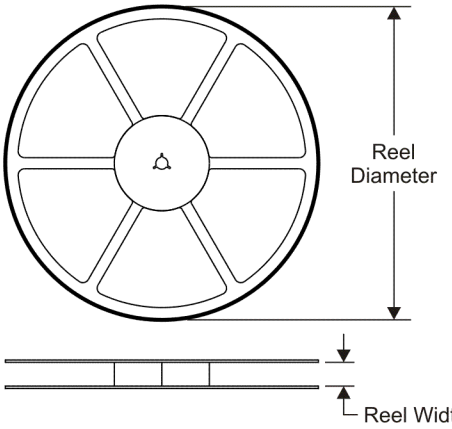
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF THS4271-EP :
- Catalog: THS4271

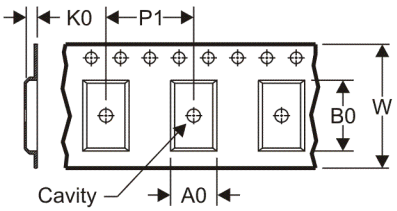
NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

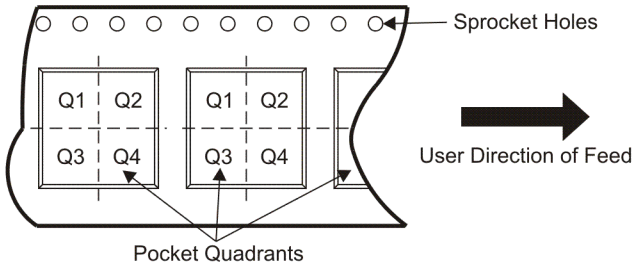


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

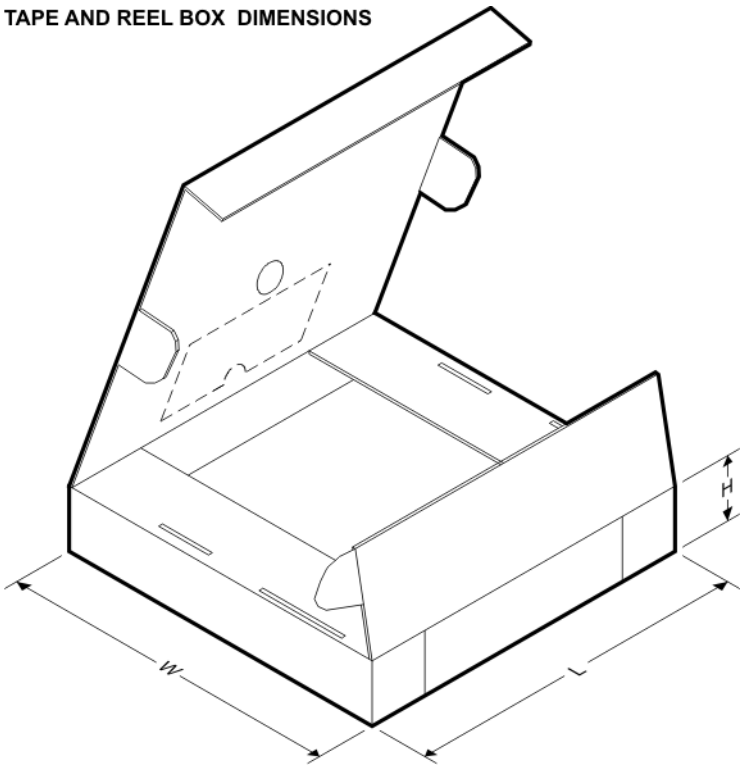
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4271MDGNREP	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.2	3.3	1.6	8.0	12.0	Q1

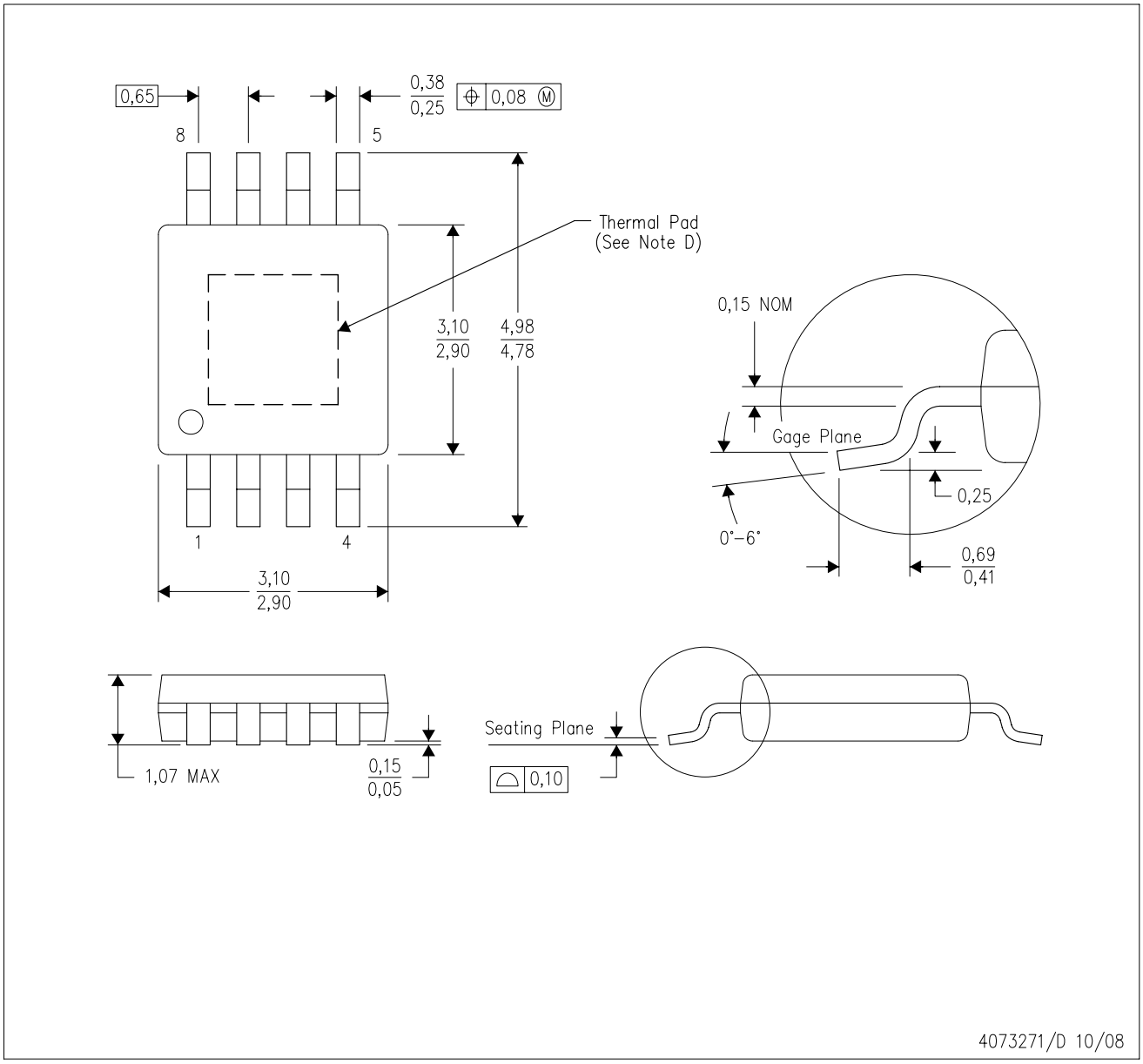
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4271MDGNREP	MSOP-PowerPAD	DGN	8	2500	338.1	340.5	21.1

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–187

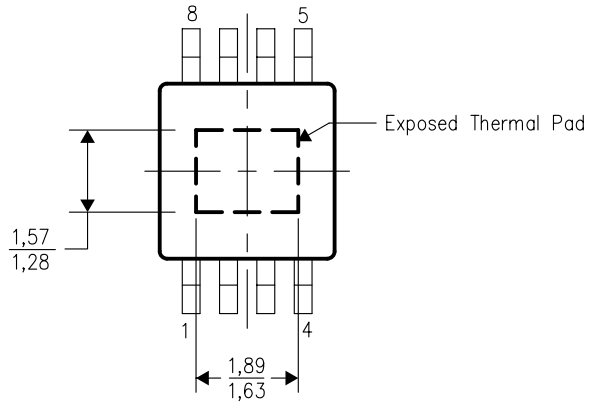
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

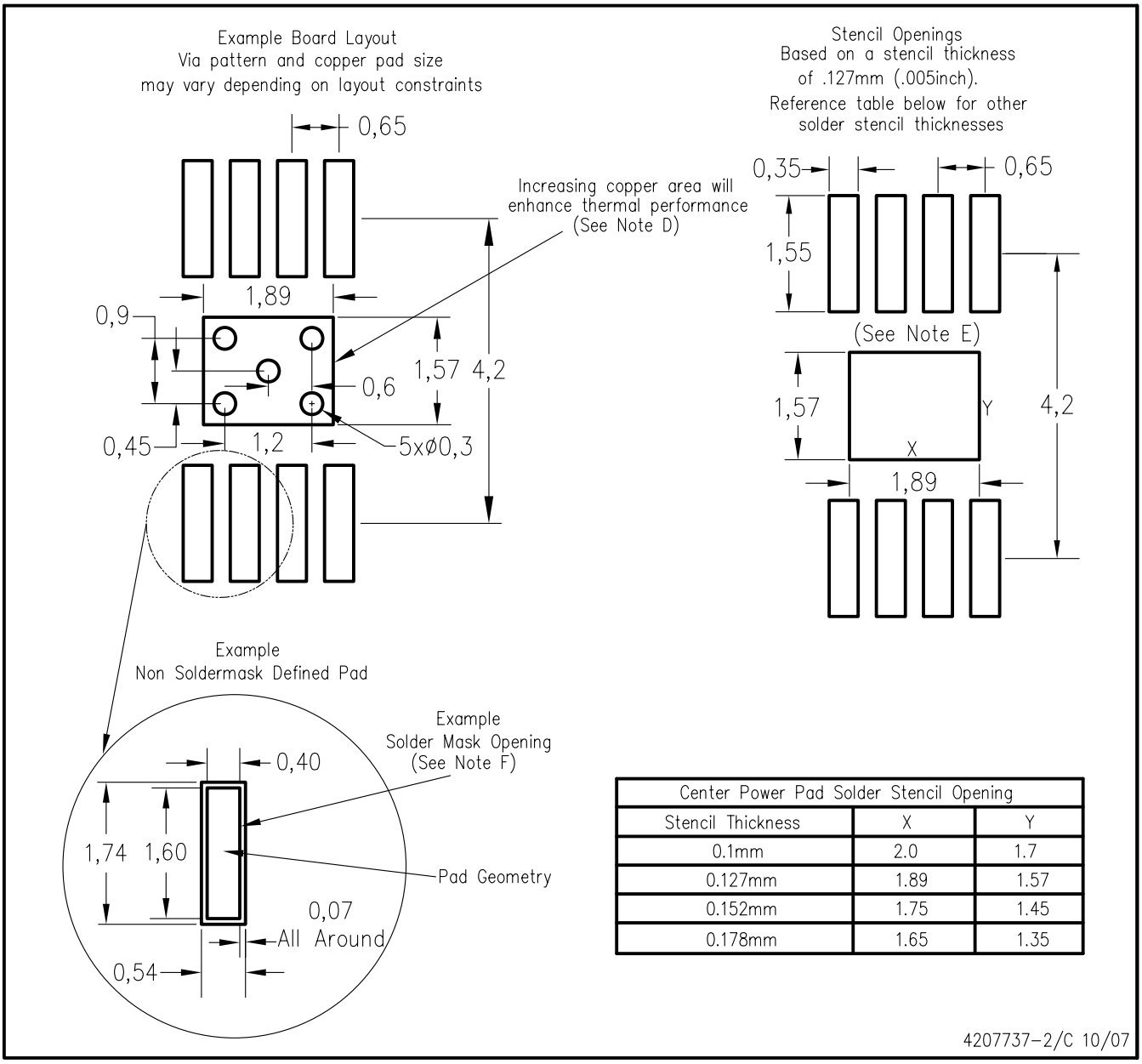


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DGN (R–PDSO–G8) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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